

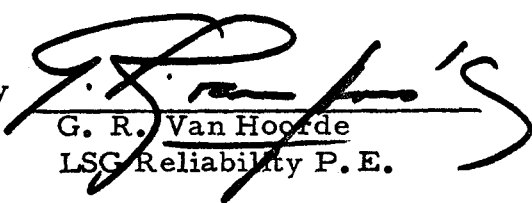


**Aerospace
 Systems Division**


Preliminary Parts Application Analysis
Lunar Surface Gravimeter Experiment

NO.	REV. NO.
ATM-979	
PAGE <u>1</u>	OF <u>114</u>
DATE <u>2/18/71</u>	

Prepared by


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LSG Reliability P.E.

Approved by


S. J. Ellison, Manager
ALSEP Reliability



**rospace
stems Division**

**Preliminary Parts Application Analysis
Lunar Surface Gravimeter Experiment**

NO. ATM-979	REV. NO.
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DATE 2/18/71	

The purpose of this ATM is to document the results of the Parts Application Analysis study conducted on the Lunar Surface Gravimeter experiment less the La Coste and Romberg sensor. This LSG represents the Bendix and ADL design electronics which uses a high degree of high reliability parts and integrated circuitry.

The stress levels shown were determined on the basis of electronic piece parts operating at their nominal values of resistance, capacitances, etc. Temperature of 50°C was used for determining device ratings. The resultant stress ratios provided the basis for determining the devices for low failure rate. In addition, all stress levels were evaluated in terms of maximum applied voltage and current levels to preclude misapplication during peak or translational periods.

The attached summary sheets (Table I) demonstrates that all parts are applied within both ALSEP and Bendix established derating criteria (ATM-241E). From the analysis it can be concluded that the LSGE electronic parts will be operating at electrical stresses well below the recommended levels for hi-rel applications.

This ATM will be updated prior to CDR.



**Aerospace
Systems Division**

Preliminary Parts Application Analysis
Lunar Surface Gravimeter Experiment

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TABLE I

LSGE DERATING SUMMARY

BxA Electronics

Quantity	Component	BxA Derating
330	Microcircuits	50 to 70% current loading or 40 to 60% fan out
345	Resistors	1 to 10% of rated power
142	Semiconductors	1 to 15% of rated power
179	Capacitors	1 to 30% of rated voltage

ADL Components

Connectors	50% of rated current
Arrestment Motor	33% of rated torque
Clutch	32% of rated torque
Mass Changing Motor	33% of rated torque
Coarse Screw Motor	12% of rated torque
Fine Screw Motor	12% of rated torque
Heater Box Heater	60% of rated current
Instrument Housing	(Night) 80% of rated current (Day) 3% of rated current

PARTS APPLICATION ANALYSIS
SUMMARY

PROJECT: LSG

DATE: 2/15

ASSEMBLY: _____

SUB ASSEMBLY: _____

SCHEMATIC NO: _____

DEVICE TYPE	TOTAL NO. USED	TOTAL FAILURE RATE	COMMENTS
CAPACITORS	179	0.086703	
RESISTORS	345	0.077868	
DIODES	96	0.176940	Combined
TRANSISTORS	46		Combined
RELAYS	16	0.064000	
TRANSFORMERS	5	0.010000	
MICROCIRCUITS	330	0.359000	
		0.774511	

TOTAL LSG FAILURE RATE 0.774511 %/1000 HOURS

MEAN-TIME-TO-FAILURE 130,000 HOURS

MISSION SUCCESS PROBABILITY _____

PARTS APPLICATION ANALYSIS

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(SEMICONDUCTORS)

PROJECT: LSG
ASSEMBLY: Board #8

SUB ASSEMBLY: Integrator

DATE: 1/20/71
SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C		AVG PWR DISSIPATION (mw)				POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION OR APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY				
			AMBIENT T _A	JUNCTION T _J	CASE T _C	RATED AT		ACTUAL T _C	ACTUAL RATED T _C	V _{CEO} RATED V	V _{CE} ACTUAL V	V _{CE0} RATED V	V _{CE} ACTUAL V	RATED V	ACTUAL V	RATE (%/1000 HRS)			SOURCE (See below)	FAILURE RATE (%/1000 HRS)	TOTAL FAILURE RATE (%/1000 HRS)		
						25°C																	
						AMBIENT T _A	CASE T _C																
CR1	SIN4942 Rectifier	Intech Corp.	50	175		4W		4W	180	4.5%					200	50	Recovery High Current		A				.0014
CR2	" "	"	50	175		4W		4W	180	4.5%					200	50	"		A				.0014
FAILURE RATE SOURCE (See Column 23) A ATM 605 C _____ B _____ D _____										NOTE: It is assumed the transient and peak power does not exceed the safe limit.										TOTAL FAILURE RATE .0028 %/1000 HRS.			

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PROJECT: ISG
ASSEMBLY: Board #7

SUB ASSEMBLY: Seismic Filter

DATE: 1/20/71

SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C		AVG PWR DISSIPATION (mw)						POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY																																																																																																					
			AMBI- ENT T _A	JUN- CTION T _J	HOT SPOT T _C	RATED AT					ACTUAL RATED 25°C Amb. or case	ACTUAL RATED T _A & T _C	V _{CEO} RATED V	V _{CB} ACTUAL V	V _{CEO} RATED V	V _{CE} ACTUAL V	RATED V	ACTUAL V			RATE (%/1000 HRS)	SOUR- CE (See below)	F ₁ FAILURE RATE (%/1000 HRS)	F ₂ FAILURE RATE (%/1000 HRS)	F ₃ FAILURE RATE (%/1000 HRS)	F ₄ FAILURE RATE (%/1000 HRS)	F ₅ FAILURE RATE (%/1000 HRS)	F ₆ FAILURE RATE (%/1000 HRS)	F ₇ FAILURE RATE (%/1000 HRS)	F ₈ FAILURE RATE (%/1000 HRS)	F ₉ FAILURE RATE (%/1000 HRS)	F ₁₀ FAILURE RATE (%/1000 HRS)	F ₁₁ FAILURE RATE (%/1000 HRS)	F ₁₂ FAILURE RATE (%/1000 HRS)	F ₁₃ FAILURE RATE (%/1000 HRS)	F ₁₄ FAILURE RATE (%/1000 HRS)	F ₁₅ FAILURE RATE (%/1000 HRS)	F ₁₆ FAILURE RATE (%/1000 HRS)	F ₁₇ FAILURE RATE (%/1000 HRS)	F ₁₈ FAILURE RATE (%/1000 HRS)	F ₁₉ FAILURE RATE (%/1000 HRS)	F ₂₀ FAILURE RATE (%/1000 HRS)	F ₂₁ FAILURE RATE (%/1000 HRS)	F ₂₂ FAILURE RATE (%/1000 HRS)	F ₂₃ FAILURE RATE (%/1000 HRS)	F ₂₄ FAILURE RATE (%/1000 HRS)	F ₂₅ FAILURE RATE (%/1000 HRS)	F ₂₆ FAILURE RATE (%/1000 HRS)	F ₂₇ FAILURE RATE (%/1000 HRS)	F ₂₈ FAILURE RATE (%/1000 HRS)	F ₂₉ FAILURE RATE (%/1000 HRS)	F ₃₀ FAILURE RATE (%/1000 HRS)	F ₃₁ FAILURE RATE (%/1000 HRS)	F ₃₂ FAILURE RATE (%/1000 HRS)	F ₃₃ FAILURE RATE (%/1000 HRS)	F ₃₄ FAILURE RATE (%/1000 HRS)	F ₃₅ FAILURE RATE (%/1000 HRS)	F ₃₆ FAILURE RATE (%/1000 HRS)	F ₃₇ FAILURE RATE (%/1000 HRS)	F ₃₈ FAILURE RATE (%/1000 HRS)	F ₃₉ FAILURE RATE (%/1000 HRS)	F ₄₀ FAILURE RATE (%/1000 HRS)	F ₄₁ FAILURE RATE (%/1000 HRS)	F ₄₂ FAILURE RATE (%/1000 HRS)	F ₄₃ FAILURE RATE (%/1000 HRS)	F ₄₄ FAILURE RATE (%/1000 HRS)	F ₄₅ FAILURE RATE (%/1000 HRS)	F ₄₆ FAILURE RATE (%/1000 HRS)	F ₄₇ FAILURE RATE (%/1000 HRS)	F ₄₈ FAILURE RATE (%/1000 HRS)	F ₄₉ FAILURE RATE (%/1000 HRS)	F ₅₀ FAILURE RATE (%/1000 HRS)	F ₅₁ FAILURE RATE (%/1000 HRS)	F ₅₂ FAILURE RATE (%/1000 HRS)	F ₅₃ FAILURE RATE (%/1000 HRS)	F ₅₄ FAILURE RATE (%/1000 HRS)	F ₅₅ FAILURE RATE (%/1000 HRS)	F ₅₆ FAILURE RATE (%/1000 HRS)	F ₅₇ FAILURE RATE (%/1000 HRS)	F ₅₈ FAILURE RATE (%/1000 HRS)	F ₅₉ FAILURE RATE (%/1000 HRS)	F ₆₀ FAILURE RATE (%/1000 HRS)	F ₆₁ FAILURE RATE (%/1000 HRS)	F ₆₂ FAILURE RATE (%/1000 HRS)	F ₆₃ FAILURE RATE (%/1000 HRS)	F ₆₄ FAILURE RATE (%/1000 HRS)	F ₆₅ FAILURE RATE (%/1000 HRS)	F ₆₆ FAILURE RATE (%/1000 HRS)	F ₆₇ FAILURE RATE (%/1000 HRS)	F ₆₈ FAILURE RATE (%/1000 HRS)	F ₆₉ FAILURE RATE (%/1000 HRS)	F ₇₀ FAILURE RATE (%/1000 HRS)	F ₇₁ FAILURE RATE (%/1000 HRS)	F ₇₂ FAILURE RATE (%/1000 HRS)	F ₇₃ FAILURE RATE (%/1000 HRS)	F ₇₄ FAILURE RATE (%/1000 HRS)	F ₇₅ FAILURE RATE (%/1000 HRS)	F ₇₆ FAILURE RATE (%/1000 HRS)	F ₇₇ FAILURE RATE (%/1000 HRS)	F ₇₈ FAILURE RATE (%/1000 HRS)	F ₇₉ FAILURE RATE (%/1000 HRS)	F ₈₀ FAILURE RATE (%/1000 HRS)	F ₈₁ FAILURE RATE (%/1000 HRS)	F ₈₂ FAILURE RATE (%/1000 HRS)	F ₈₃ FAILURE RATE (%/1000 HRS)	F ₈₄ FAILURE RATE (%/1000 HRS)	F ₈₅ FAILURE RATE (%/1000 HRS)	F ₈₆ FAILURE RATE (%/1000 HRS)	F ₈₇ FAILURE RATE (%/1000 HRS)	F ₈₈ FAILURE RATE (%/1000 HRS)	F ₈₉ FAILURE RATE (%/1000 HRS)	F ₉₀ FAILURE RATE (%/1000 HRS)	F ₉₁ FAILURE RATE (%/1000 HRS)	F ₉₂ FAILURE RATE (%/1000 HRS)	F ₉₃ FAILURE RATE (%/1000 HRS)	F ₉₄ FAILURE RATE (%/1000 HRS)	F ₉₅ FAILURE RATE (%/1000 HRS)	F ₉₆ FAILURE RATE (%/1000 HRS)	F ₉₇ FAILURE RATE (%/1000 HRS)	F ₉₈ FAILURE RATE (%/1000 HRS)	F ₉₉ FAILURE RATE (%/1000 HRS)	F ₁₀₀

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PARTS APPLICATION ANALYSIS

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(SEMICONDUCTORS)

PROJECT: LSG
ASSEMBLY: Board 4 and 5SUB ASSEMBLY: Screw Servo Central &DATE: 1/20/71
SCHEMATIC NO: _____

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	M A N U F A C T U R E R	MAX. TEMP °C		AVG PWR DISSIPATION (mw)				POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY							
			A M B I E N T T _A	J U N C T I O N T _J	A C T U A L H O T S P O T T _C	RATED AT				A C T U A L R A T E D T _A or T _C (Amb. or case)	V _{CB0} R A T E D V	V _{CB} A C T U A L V	V _{CS0} R A T E D V	V _{CE} A C T U A L V	R A T E D V	A C T U A L V			R A T E (%/1000 HRS)	S O U R C E R A T E (%/1000 HRS) (See below)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	C O T U R A N T P E R T Y P E (%/1000 HRS)	T O T A L F A I L U R E R A T E (%/1000 HRS)		
						25°C		A M B I E N T T _A	A C T U A L T _C																A C T U A L T _C	A C T U A L T _C
						A M B I E N T T _A	C A S E T _C																			
12	SIN #4942 Sil Rectifier		50	175		4W		4W	180	4.5%					200	50	Recovery High Current		A						.0160	
4	SIN 91613 Sil Switch			200		250		214	<1	<1%					75	12	Switch								.0020	
4	transistor Silicon PNP S2N2907A			200		400		343	<1	<1%	60		60				Switching								.0078	
4	transistor Silicon NPN S2N910			200		500		242	<1	<1%	100		60				Switching								.0078	
18 ATM ⁷ FAILURE RATE SOURCE (See Column 23) A _____ C _____ B _____ D _____										19 NOTE: It is assumed the transient and peak power does not exceed the safe limit.										20 TOTAL FAILURE RATE - .0336 %/1000 HRS.						

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(SEMICONDUCTORS)

PROJECT: LSG
ASSEMBLY: Board 6

SUB ASSEMBLY: Mass Change Servo.

DATE: 1/20/71
SCHEMATIC NO:

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C		AVG PWR DISSIPATION (mw)				POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY										
			AMBI- ENT TA	RATED TJ	JUNCTION TJ	ACTUAL Tc	CASE Tc	RATED AT				ACTUAL RATED 25°C Ambor case	ACTUAL RATED TA or TC	VCBO RATED V	VCB ACTUAL V	VCEO RATED V			VCE ACTUAL V	RA RATED V	AC ACTUAL V	RATE (%/1000 HRS)	S OUR- CE (See below)	F AIL- URE R ATE (%/1000 HRS)	F AIL- URE R ATE (%/1000 HRS)	F AIL- URE R ATE (%/1000 HRS)	C O U N- T PER TYPE	TOTAL FAILURE RATE (%/1000 HRS)	
								25°C		AMBI- ENT TA	ACTUAL Tc																		CASE Tc
								AMBI- ENT TA	CASE Tc																				
CR2	SIN 4942 Sil Switch		50	175		4W		4W		180	4.5%						200	50	Recovery High Current			A					.0014		
CR3																													
CR8																													
CR9																													
CR10	SIN 4942 Sil Rectifier	Sem- Tech Cap																											
CR11																													
CR12																													
CR13																													
CR14																													

FAILURE RATE SOURCE (See Column 23)

A ATM 605

B

C

D

NOTE: R is assumed the transient and peak power does not exceed the safe limit.

TOTAL FAILURE RATE 0.0126 %/1000 HRS.

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PARTS APPLICATION ANALYSIS

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(SEMICONDUCTORS)

PROJECT: LSG

ASSEMBLY: Board 6

SUB ASSEMBLY: Mass Change Servo

DATE: 1/20/71

SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C		AVG PWR DISSIPATION (mw)						POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY												
			AMBI- ENT TA	JUN- CTION TJ	ACTU- AL TC	CASE HOT SPOT TC	RATED AT		ACTU- AL TA	ACTU- AL TC	ACTU- AL TA	ACTU- AL TC	ACTU- AL TA	ACTU- AL TC	VCBO RATED V	VCB ACTU- AL V	VCEO RATED V	VCE ACTU- AL V			RATED V	ACTU- AL V	RATE (%/1000 HRS)	SOUR- CE (See below)	FAL- TURE RATE (%/1000 HRS)	FAL- TURE RATE (%/1000 HRS)	FAL- TURE RATE (%/1000 HRS)	FAL- TURE RATE (%/1000 HRS)	TOTAL FAILURE RATE (%/1000 HRS)				
							25°C	CASE																						25°C	CASE	25°C	CASE
CR15	SIN 4942 Sil Rectifier	SGS CORP	50	175		4W		4W		180	4.5%						200	50	Recovery High Current								.0014						
CR4	SIN 751A Sil Zener	DKK SON		175		400		400		24	5.8%								Low Voltage Regulator								.00127						
CR5																																	
CR6	IN4579A Sil Zener	Dickson Mfg								35	9%								Reference Zener														
CR7	IN5304 Sil Current Reg	Dickson Mfg		200		600		600		20	3.3%								Current Regulator								.00059						
Q1	Transistor Sil PNP S2N2907A			200		400		343					60		60				Switching														
Q2																																	
Q3																																	
Q6																																	

20 FAILURE RATE SOURCE (See Column 23)

A ATM 605 C _____

B _____ D _____

21 NOTE: It is assumed the transient and peak power does not exceed the safe limit.

22 TOTAL FAILURE RATE .00816 %/1000 HRS.

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(SEMICONDUCTORS)

LSG

Board 6

SUB ASSEMBLY: Mass change servo

1/20/71

SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C		AVG PWR DISSIPATION (mw)				POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY					
			AMBI- ENT T _A	JUN- CTION T _J	CASE HOT SPOT T _C	RATED AT				ACTUAL RATED 25 °C Amb.or case)	ACTUAL T _A or T _C	V _{CB0} RATED V	V _{CB} ACTUAL V	V _{CB0} RATED V	V _{CE} ACTUAL V	RATED V			ACTUAL V	RATE (%/1000 HRS)	SO- LID- STATE R ₁ R ₂ R ₃ R ₄ R ₅ R ₆ R ₇ R ₈ R ₉ R ₁₀ R ₁₁ R ₁₂ R ₁₃ R ₁₄ R ₁₅ R ₁₆ R ₁₇ R ₁₈ R ₁₉ R ₂₀ R ₂₁ R ₂₂ R ₂₃ R ₂₄ R ₂₅ R ₂₆ R ₂₇ R ₂₈ R ₂₉ R ₃₀ R ₃₁ R ₃₂ R ₃₃ R ₃₄ R ₃₅ R ₃₆ R ₃₇ R ₃₈ R ₃₉ R ₄₀ R ₄₁ R ₄₂ R ₄₃ R ₄₄ R ₄₅ R ₄₆ R ₄₇ R ₄₈ R ₄₉ R ₅₀ R ₅₁ R ₅₂ R ₅₃ R ₅₄ R ₅₅ R ₅₆ R ₅₇ R ₅₈ R ₅₉ R ₆₀ R ₆₁ R ₆₂ R ₆₃ R ₆₄ R ₆₅ R ₆₆ R ₆₇ R ₆₈ R ₆₉ R ₇₀ R ₇₁ R ₇₂ R ₇₃ R ₇₄ R ₇₅ R ₇₆ R ₇₇ R ₇₈ R ₇₉ R ₈₀ R ₈₁ R ₈₂ R ₈₃ R ₈₄ R ₈₅ R ₈₆ R ₈₇ R ₈₈ R ₈₉ R ₉₀ R ₉₁ R ₉₂ R ₉₃ R ₉₄ R ₉₅ R ₉₆ R ₉₇ R ₉₈ R ₉₉ R ₁₀₀ R ₁₀₁ R ₁₀₂ R ₁₀₃ R ₁₀₄ R ₁₀₅ R ₁₀₆ R ₁₀₇ R ₁₀₈ R ₁₀₉ R ₁₁₀ R ₁₁₁ R ₁₁₂ R ₁₁₃ R ₁₁₄ R ₁₁₅ R ₁₁₆ R ₁₁₇ R ₁₁₈ R ₁₁₉ R ₁₂₀ R ₁₂₁ R ₁₂₂ R ₁₂₃ R ₁₂₄ R ₁₂₅ R ₁₂₆ R ₁₂₇ R ₁₂₈ R ₁₂₉ R ₁₃₀ R ₁₃₁ R ₁₃₂ R ₁₃₃ R ₁₃₄ R ₁₃₅ R ₁₃₆ R ₁₃₇ R ₁₃₈ R ₁₃₉ R ₁₄₀ R ₁₄₁ R ₁₄₂ R ₁₄₃ R ₁₄₄ R ₁₄₅ R ₁₄₆ R ₁₄₇ R ₁₄₈ R ₁₄₉ R ₁₅₀ R ₁₅₁ R ₁₅₂ R ₁₅₃ R ₁₅₄ R ₁₅₅ R ₁₅₆ R ₁₅₇ R ₁₅₈ R ₁₅₉ R ₁₆₀ R ₁₆₁ R ₁₆₂ R ₁₆₃ R ₁₆₄ R ₁₆₅ R ₁₆₆ R ₁₆₇ R ₁₆₈ R ₁₆₉ R ₁₇₀ R ₁₇₁ R ₁₇₂ R ₁₇₃ R ₁₇₄ R ₁₇₅ R ₁₇₆ R ₁₇₇ R ₁₇₈ R ₁₇₉ R ₁₈₀ R ₁₈₁ R ₁₈₂ R ₁₈₃ R ₁₈₄ R ₁₈₅ R ₁₈₆ R ₁₈₇ R ₁₈₈ R ₁₈₉ R ₁₉₀ R ₁₉₁ R ₁₉₂ R ₁₉₃ R ₁₉₄ R ₁₉₅ R ₁₉₆ R ₁₉₇ R ₁₉₈ R ₁₉₉ R ₂₀₀ R ₂₀₁ R ₂₀₂ R ₂₀₃ R ₂₀₄ R ₂₀₅ R ₂₀₆ R ₂₀₇ R ₂₀₈ R ₂₀₉ R ₂₁₀ R ₂₁₁ R ₂₁₂ R ₂₁₃ R ₂₁₄ R ₂₁₅ R ₂₁₆ R ₂₁₇ R ₂₁₈ R ₂₁₉ R ₂₂₀ R ₂₂₁ R ₂₂₂ R ₂₂₃ R ₂₂₄ R ₂₂₅ R ₂₂₆ R ₂₂₇ R ₂₂₈ R ₂₂₉ R ₂₃₀ R ₂₃₁ R ₂₃₂ R ₂₃₃ R ₂₃₄ R ₂₃₅ R ₂₃₆ R ₂₃₇ R ₂₃₈ R ₂₃₉ R ₂₄₀ R ₂₄₁ R ₂₄₂ R ₂₄₃ R ₂₄₄ R ₂₄₅ R ₂₄₆ R ₂₄₇ R ₂₄₈ R ₂₄₉ R ₂₅₀ R ₂₅₁ R ₂₅₂ R ₂₅₃ R ₂₅₄ R ₂₅₅ R ₂₅₆ R ₂₅₇ R ₂₅₈ R ₂₅₉ R ₂₆₀ R ₂₆₁ R ₂₆₂ R ₂₆₃ R ₂₆₄ R ₂₆₅ R ₂₆₆ R ₂₆₇ R ₂₆₈ R ₂₆₉ R ₂₇₀ R ₂₇₁ R ₂₇₂ R ₂₇₃ R ₂₇₄ R ₂₇₅ R ₂₇₆ R ₂₇₇ R ₂₇₈ R ₂₇₉ R ₂₈₀ R ₂₈₁ R ₂₈₂ R ₂₈₃ R ₂₈₄ R ₂₈₅ R ₂₈₆ R ₂₈₇ R ₂₈₈ R ₂₈₉ R ₂₉₀ R ₂₉₁ R ₂₉₂ R ₂₉₃ R ₂₉₄ R ₂₉₅ R ₂₉₆ R ₂₉₇ R ₂₉₈ R ₂₉₉ R ₃₀₀ R ₃₀₁ R ₃₀₂ R ₃₀₃ R ₃₀₄ R ₃₀₅ R ₃₀₆ R ₃₀			

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PARTS APPLICATION ANALYSIS

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(SEMICONDUCTORS)

PROJECT: ISG
ASSEMBLY: Board 5SUB ASSEMBLY: Caging ControlDATE: 1/20/71
SCHEMATIC NO: _____

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C		AVG PWR DISSIPATION (mw)						POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION OR APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY					
			AMBI- ENT TA	JUNC- TION TJ	CASE Tc	RATED AT				ACTUAL Tc	ACTUAL RATED 25°C Amb.or case	ACTUAL Tc	VBO RATED V	VCB ACTUAL V	VCEQ RATED V	VCE ACTUAL V	RATED V	ACTUAL V			RATE (%/1000 HRS)	SOUR- CE (See below)	FAC- TOR RPL TYPE	TOTAL FAILURE RATE (%/1000 HRS)		
						25°C		ACTUAL Tc	ACTUAL Tc																ACTUAL Tc	
						AMBI- ENT TA	CASE Tc																			
CR2	SIN 916B Sil Switch	50M 60197	50	200	250		214		1	1%						75		Switching		A		.0005				
CR3																										
CR5																										
CR6																										
CR4	SIN 4942 Sil Rectifier	85M 03895		175	4W		4W		180	4.5%						200	50	Recovery High Current				.0014				
CR7																										
CR8																										
CR1	SIN 963B Sil Zener	85M 01309		175	400		400		15	4%						20		DC Regulator				.00127				
Q2	Transistor Sil NPN ZN930A			200	500		417		2	1%		60	60					Low level low amplifier				.00195				
FAILURE RATE SOURCE (See Column 23)					NOTE: It is assumed the transient and peak power does not exceed the safe limit.										TOTAL FAILURE RATE <u>.00042</u> %/1000 HRS.											
A <u>ATM 605</u> C _____																										
B _____ D _____																										

FORM

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(SEMICONDUCTORS)

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ASSEMBLY: Board 5

SUB ASSEMBLY: Caging Control

DATE: 1/20/21

SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	M A N U F A C T U R E R	MAX. TEMP °C		AVG PWR DISSIPATION (mw)						POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY						
			A M B I E N T T _A	J U N C T I O N T _J	A C T U A L N O T S P O T T _C	RATED AT						ACTUAL RATED 25°C Amb.or case) T ₂₅	ACTUAL RATED T _A or T _C	V _{CB0} R A T E D V	V _{CB} A C T U A L V	V _{CE0} R A T E D V	V _{CE} A C T U A L V	R A T E D V			A C T U A L V	RATE (%/1000 HRS) (See below)	F A U L T I T A L	F A I L U R E R A T E (%/1000 HRS)	T O T A L F A I L U R E R A T E (%/1000 HRS)		
						25°C		A M B I E N T T _A	C A S E T _C	A C T U A L T _T	A C T U A L T _C																
						A M B I E N T T _A	C A S E T _C																				
Q1	transistor Fet 3N 171	micron	50	200		300		257.9		3	1%							low PWR Switching		A				.00195			
Q4	transistor Sil PNP S2N 2905A	66109 IND	50	200		600		514.2		6	1%	60		60				High Speed Switching		A							
Q3	transistor Sil PNP SM2N2907A	86109 IND	50	200		400		343		8	2%	60		60				"		A							

rate

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(SEMICONDUCTORS)

PROJECT: LSG

DATE: 1/20/71

ASSEMBLY: Board 14

SUB ASSEMBLY: Shaft Encodes elect.

SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C			AVG PWR DISSIPATION (mw)				POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY						
			AMBIENT T _A	RATED T _J	JUNCTION HOT SPOT T _C	RATED AT				ACTUAL T _A or T _C	ACTUAL RATED 25°C Amb. or case	V _{CEO} RATED V	V _{CB} ACTUAL V	V _{CEO} RATED V	V _{CE} ACTUAL V	RATED V	ACTUAL V			RATE (%/1000 HRS)	S O U R C E (See below)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	T O T A L F A I L U R E R A T E (%/1000 HRS)		
						25°C		ACTUAL T _A	ACTUAL T _C																ACTUAL T _A or T _C	
						AMBIENT T _A	CASE T _C																			
Q1	transistor Sil PNP S2N2905A		50	200	600	514.2	6	1%		60		60					High Speed Switching			A				.00195		
Q2	transistor Sil NPN S2N222A		50	200	500	417	10	2%		75		40					medium speed switching			A				.00195		
FAILURE RATE SOURCE (See Column 23) A ATM 605 C _____ B _____ D _____										NOTE: R is assumed the transient and peak power does not exceed the safe limit.										TOTAL FAILURE RATE .00390 %/1000 HRS.						

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DATE: 1/20/71
SCHEMATIC NO:

ASSEMBLY: Board 15

SUB ASSEMBLY: Instrument Housing Temp.
Control

(Semiconductors)

CMT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C		AVG PWR DISSIPATION (mw)						POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY						
			AMBIENT T _A	JUNCTION T _J	HOT SPOT T _C	RATED AT						ACTUAL RATED 25°C (Amb.or case)	ACTUAL RATED T _A or T _C	V _{CB0} V	V _{CB} V	V _{CE0} V	V _{CE} V	RATED V			ACTUAL V	RATE (%/1000 HRS)	SOURCE REALISER (See below)	F A I L U R E P E R T Y P E (#/1000 HRS)	TOTAL FAILURE RATE		
						25°C		CASE T _C	AMBIENT T _A	JUNCTION T _J	HOT SPOT T _C																
						A	B																				
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
Q1	transistor Sil PNP SM2N2907A		50	200		400		343	10	2.5%	60		60					high speed switching		A						.00195	
Q2	transistor Sil NPN S2N930					500		417	5	1%								low level "level amplifier"									
Q3	transistor Sil PNP S2N3720					1W		857	20	2%	60		60					High current switching									
Q4	transistor Sil PNP SM2N2905A					600		514	6	1%								Series Reg									
CR1	IN5292 Current Reg	mdm				660		600	30	5%								current Reg								.00059	
CR2	IN4568A Volt Ref	dobson		175		250		250	24	9%								voltage ref								.0007	
CR5	SIN 91613 Sil Switch			200		250		214	1	1%							75	12	Switching							.0005	
CR6																											

FAILURE RATE SOURCE (See Column 23)
A — ATM 605 C —
B — D —

NOTE: It is assumed the transient and peak power does not exceed the safe limit.

TOTAL FAILURE RATE — .01204 — %/1000 HRS.

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(SEMICONDUCTORS)

PROJECT: LSG
ASSEMBLY: Board 15

SUB ASSEMBLY: Instrument Housing Temp Control

DATE: 1/20/71
SCHEMATIC NO:

(Semiconductors)

CMT SYM NO.	TYPE DESIGNATION, SEMI-CONDUCTOR, POLARITY	M A N U F A C T U R E R	MAX. TEMP °C		AVG PWR DISSIPATION (mw)						POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Def(ce))	FOR RELIABILITY USE ONLY							
			A M B I E N T T _A	J U N C T I O N T _J	C A S E T _C	RATED AT		A M B I E N T T _A	C A S E T _C	A C T U A L T _C	A C T U A L R A T E D 25°C (Amb.or case)	A C T U A L R A T E D T _A OF T _C	V C B O R A T E D V	V C B A C T U A L V	V C E O R A T E D V	V C E A C T U A L V	R A T E D V	A C T U A L V			R A T E D 25°C HRS	S O U R C E (See below)	F A I L U R E R A T E R HRS	F A I L U R E R A T E R HRS	C O U N T P E R T Y P E	T O T A L F A I L U R E R A T E R HRS		
						25°C																						
						A M B I E N T	C A S E																					
						T _A	T _C																					
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25				
CR8	SIN 4942 Sil Rectifier	Scintec	50	175		4W		4W		18G	4.5%						200	50	Relay coil Suppre.						.0014			
CR9		↓		↓		↓		↓		↓	↓						↓	↓	↓						↓			
CR10	LM103-2.4/883 Volt Ref	haxma semi		150		250		220		24	10.8%								Voltage Reg						.0007			
CR11		↓	↓	↓		↓		↓		↓	↓								↓						↓			

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(SEMICONDUCTORS)

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ASSEMBLY: Board #10

SUB ASSEMBLY: Power Converter

SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	M A N U F A C T U R E R	MAX. TEMP °C		AVG PWR DISSIPATION (mw)				POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY							
			A M B I E N T T _A	J U N C T I O N T _J	C A S E R O T S P O T T _C	RATFDAT				A C T U A L R A T E D 25°C Amb.or case	A C T U A L R A T E D T _A or T _C	V C B O R A T E D V	V C B R A T E D V	V C B O R A T E D V	V C E R A T E D V	R A T E D V			A C T U A L V	R A T E (%/1000 HRS)	S U R V I V A L R A T E (See below %/1000 HRS)	F U N C T I O N A L R A T E (%/1000 HRS)	T O T A L P E R T Y P E	T O T A L F A I L U R E R A T E (%/1000 HRS)		
						A M B I E N T T _A	C A S E T _C	A C T U A L T _A	A C T U A L T _C																	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
CR1	IN4568A Sil Zener	Dick- son	50	175		250		250	8	<1%								5	Volt- age Ref.		A					.0007
CR2	SIN4942 Sil Rectifier	Sem- tec		175		4w		4w	3	<1%							200	50	Recovery High Current							.0014
CR3	" "								5	"								50								
CR4	" "								40	"								40								
CR5	" "								200	1%								40								
CR6	" "								200	"								40								
CR7	" "								40	<1%								40								
CR8	" "								5	"								50								
CR9 & CR10	" "								150	1%								15								

FAILURE RATE SOURCE (See Column 23)
A ATM 605 C _____
B _____ D _____

NOTE: R is assumed the transient and peak power does not exceed the safe limit.

TOTAL FAILURE RATE .0119 %/1000 HRS.

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(SEMICONDUCTORS)

PROJECT: LSG

ASSEMBLY: Board #10

SUB ASSEMBLY: Power Converter

DATE: 1/20/71

SCHEMATIC NO:

(Semiconductors)

CMT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	M A N U F A C T U R E R	MAX. TEMP °C		AVG PWR DISSIPATION (mw)						POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY																																																																																																																							
			A M B I E N T T _A	J U N C T I O N T _J	C A S E H O T S P O T T _C	RATED AT						A C T U A L R A T E D 25°C (Amb.or case)	A C T U A L R A T E D T _A or T _C	V C B O R A T E D V	V C B A C T U A L V	V C E O R A T E D V	V C E A C T U A L V	R A T E D V			A C T U A L V	R A T E D %	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000 HRS)	F A I L U R E R A T E (%/1000

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(SEMICONDUCTORS)

PROJECT: LSG
ASSEMBLY: Board #8

SUB ASSEMBLY: Stabilized Oscillator

DATE: 1/20/71

SCHEMATIC NO:

(Semiconductors)

CXT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	M A N U F A C T U R E R	MAX. TEMP °C			AVG PWR DISSIPATION (mw)					POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION OR APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY						
			A M B I E N T T _A	J U N C T I O N T _J	C A S E H O T S P O T T _C	RATED AT					ACTUAL RATED T _A & T _C	ACTUAL RATED T _A & T _C	V _{CEO} R A T E D V	V _{CB} A C T U A L V	V _{CE0} R A T E D V	V _{CE} A C T U A L V	R A T E D V	A C T U A L V			RATE (%/1000 HRS)	S O U R C E (See below)	F A I L U R E R A T E (%/1000 HRS)	M U L T I P L I C A T I O N F A C T O R	T O T A L F A I L U R E R A T E (%/1000 HRS)		
						25°C																					
						A M B I E N T T _A	C A S E T _C	A C T U A L T _A	A C T U A L T _C	A C T U A L T _A																	
	IN5299 Current Reg.	MOT	50	200		660		600		30	5%										A			.00059			
	IN4574A	Dick- son		175		250		250		24	9.6 %													.0021			
4	SIN914 Signal		50	200		250		214		10	2.1 %						75	12	Signal		A			.00236			
FAILURE RATE SOURCE (See Column 23) A ATM 605 C _____ B _____ D _____						NOTE: R is assumed the transient and peak power does not exceed the safe limit.										TOTAL FAILURE RATE .00505 %/1000 HRS.											

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(SEMICONDUCTORS)

PROJECT: LSG
ASSEMBLY: Board #8

SUB ASSEMBLY: Stabilized Oscillator

DATE: 1/20/71
SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	M A N U F A C T U R E R	MAX. TEMP °C		AVG PWR DISSIPATION (mW)						POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY					
			A M B I E N T T _A	J U N C T I O N T _J	C A S E T _C	RATED AT			A C T U A L T _A	A C T U A L RATED 25°C (Amb or case)	A C T U A L RATED T _A or T _C	V _{CB0} R A T E D V	V _{CB} A C T U A L V	V _{CE0} R A T E D V	V _{CE} A C T U A L V	R A T E D V	A C T U A L V	R A T E (/1000 HRS)			S O U R C E R A T E (/1000 HRS) (See below)	F A I L U R E R A T E (/1000 HRS)	F A I L U R E R A T E (/1000 HRS)	T O T A L F A I L U R E R A T E (/1000 HRS)		
						25°C																				
						A M B I E N T T _A	C A S E T _C	A C T U A L T _A																		
CR ₁	SIN4942 Rectifier		50	175		4W		4W		180	4.5 %					200	50		Receiver High Current		A				.0014	
CR ₂	SIN4942 Rectifier		50	175		4W		4W		180	4.5 %					200	50				A				.0014	
20 FAILURE RATE SOURCE (See Column 23) A ATM 605 C _____ B _____ D _____										21 NOTE: It is assumed the transient and peak power does not exceed the safe limit.										22 TOTAL FAILURE RATE .0028 %/1000 HRS.						

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(SEMICONDUCTORS)

PROJECT: LSG

DATE: 1/20/71

ASSEMBLY: Board #8

SUB ASSEMBLY: Post-Ampl.

SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C			AVG PWR DISSIPATION (mw)					POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY					
			AMBIENT T _A	JUNCTION T _J	CASE HOT SPOT T _C	RATED AT				ACTUAL RATED 25°C Amb. or case	ACTUAL RATED T _A or T _C	V _{CEO} RATED V	V _{CB} ACTUAL V	V _{CEO} RATED V	V _{CE} ACTUAL V	RATED V	ACTUAL V	RATE (%/1000 HRS)			SOIL- ING RATE (%/1000 HRS)	F ₁ F ₂ F ₃ F ₄ F ₅ F ₆ F ₇ F ₈ F ₉ F ₁₀ F ₁₁ F ₁₂ F ₁₃ F ₁₄ F ₁₅ F ₁₆ F ₁₇ F ₁₈ F ₁₉ F ₂₀ F ₂₁ F ₂₂ F ₂₃ F ₂₄ F ₂₅ F ₂₆ F ₂₇ F ₂₈ F ₂₉ F ₃₀ F ₃₁ F ₃₂ F ₃₃ F ₃₄ F ₃₅ F ₃₆ F ₃₇ F ₃₈ F ₃₉ F ₄₀ F ₄₁ F ₄₂ F ₄₃ F ₄₄ F ₄₅ F ₄₆ F ₄₇ F ₄₈ F ₄₉ F ₅₀ F ₅₁ F ₅₂ F ₅₃ F ₅₄ F ₅₅ F ₅₆ F ₅₇ F ₅₈ F ₅₉ F ₆₀ F ₆₁ F ₆₂ F ₆₃ F ₆₄ F ₆₅ F ₆₆ F ₆₇ F ₆₈ F ₆₉ F ₇₀ F ₇₁ F ₇₂ F ₇₃ F ₇₄ F ₇₅ F ₇₆ F ₇₇ F ₇₈ F ₇₉ F ₈₀ F ₈₁ F ₈₂ F ₈₃ F ₈₄ F ₈₅ F ₈₆ F ₈₇ F ₈₈ F ₈₉ F ₉₀ F ₉₁ F ₉₂ F ₉₃ F ₉₄ F ₉₅ F ₉₆ F ₉₇ F ₉₈ F ₉₉ F ₁₀₀ F ₁₀₁ F ₁₀₂ F ₁₀₃ F ₁₀₄ F ₁₀₅ F ₁₀₆ F ₁₀₇ F ₁₀₈ F ₁₀₉ F ₁₁₀ F ₁₁₁ F ₁₁₂ F ₁₁₃ F ₁₁₄ F ₁₁₅ F ₁₁₆ F ₁₁₇ F ₁₁₈ F ₁₁₉ F ₁₂₀ F ₁₂₁ F ₁₂₂ F ₁₂₃ F ₁₂₄ F ₁₂₅ F ₁₂₆ F ₁₂₇ F ₁₂₈ F ₁₂₉ F ₁₃₀ F ₁₃₁ F ₁₃₂ F ₁₃₃ F ₁₃₄ F ₁₃₅ F ₁₃₆ F ₁₃₇ F ₁₃₈ F ₁₃₉ F ₁₄₀ F ₁₄₁ F ₁₄₂ F ₁₄₃ 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PROJECT: LSG

DATE: 1/20/71

ASSEMBLY: Motor Drive Control

SUB ASSEMBLY: Tilt-Servo Control

SCHEMATIC NO:

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANU- FACTURER	MAX. TEMP °C						AVG PWR DISSIPATION (mw)							POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Def loc)	FOR RELIABILITY USE ONLY							
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								AMBI- ENT TA	CASE TC																								
CR1 thru CR8	SIN 4942 Rectifier	Semtec	50	175		4W		4W		180	4.5 %						200	50					A		.0014								
CR1 thru CR17	SIN4942 Rectifier	"		175		4W		4W		180	4.5 %						200	50	"						.0014								
CR9	SIN916B Sil. Switch	T.I.		200		250		214		<1	<1%						75	12	Switching						.0005								
CR10	SIN916B Sil. Switch	"				250		214		<1	<1%						75	12	"						.0005								
Q1	Transistor Sil. PNP S2N2907A	T.I. MOT Ray				400		343		20	5%			60		60			High Speed Switching						.00195								
Q3	Transistor Sil. PNP S2N2907A	"																	"														
Q5	Transistor Sil. PNP S2N2907A	"																	"														
Q7	Transistor Sil. PNP S2N2907A	T.I. MOT Ray	50	200		400		343		20	5%			60		60			High Speed Switching						.00195								

FAILURE RATE SOURCE (See Column 23)
A ATM 605 C _____
B _____ D _____

NOTE: It is assumed the transient and peak power does not exceed the safe limit.

TOTAL FAILURE RATE .01160 %/1000 HRS.

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(SEMICONDUCTORS)

PROJECT: LSG
ASSEMBLY: Board #4

SUB ASSEMBLY: Tilt Servo Control

DATE: 1/20/71

SCHEMATIC NO:

(Semiconductors)

Ckt SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C			AVG PWR DISSIPATION (mw)				POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY					
			AMBIENT T _A	JUNCTION T _J	CASE T _C	RATED AT				ACTUAL RATED PWR Amb or case	ACTUAL RATED PWR T _A or T _C	V _{CB0} RATED V	V _{CB} ACTUAL V	V _{CE0} RATED V	V _{CE} ACTUAL V	RATED V	ACTUAL V			RATE (%/1000 HRS) (See below)	SO URCE R ATE R (%/1000 HRS)	F A U L T R ATE (%/1000 HRS)	F A U L T R ATE (%/1000 HRS)	T O T A L F A I L U R E R ATE (%/1000 HRS)	
						35°C																			
						AMBIENT T _A	CASE T _C	ACTUAL T _A	ACTUAL T _C																
Q ₂	Transistor Sil. NPN S2N910	T.I. Ray	50	200		500		428.5		50	10%		100		60			Switch- ing		A				.00195	
Q ₄	Transistor Sil. NPN S2N910	"																							
Q ₆	Transistor Sil. NPN S2N910	"																							
Q ₈	Transistor Sil. NPN S2N910	T.I. Ray	50	200		500		428.5		50	10%		100		60			Switch- ing		A				.00195	
19 FAILURE RATE SOURCE (See Column 23) A ATM 605 C _____ B _____ D _____										20 NOTE: It is assumed the transient and peak power does not exceed the safe limit.										21 TOTAL FAILURE RATE .00780 %/1000 HRS.					

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PROJECT: LSG
ASSEMBLY: Board #15

SUB ASSEMBLY: Temp. Monitor

DATE: 1/20/71

SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	M A N U F A C T U R E R	MAX. TEMP °C		AVG PWR DISSIPATION (mw)				POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY							
			A M B I E N T T _A	A C T U A L R A T E D T _J	J U N C T I O N T _J	C A S E H O T S P O T T _C	RATED AT				A C T U A L R A T E D 25°C (Amb.or case)	A C T U A L R A T E D T _A & T _C	V _{CB0} R A T E D V	V _{CB} A C T U A L V	V _{CEO} R A T E D V	V _{CE} A C T U A L V			R A T E D V	A C T U A L V	R A T E (%/1000 HRS)	S O U R C E (See below)	F U L T I P L I C A T I O N R A T E (%/1000 HRS)	T O T A L P E R T Y P E	T O T A L F A I L U R E R A T E (%/1000 HRS)	
							25°C		A M B I E N T T _A	C A S E T _C																A C T U A L R A T E D T _A & T _C
							A M B I E N T T _A	C A S E T _C																		
CR ₃	SIN916B Sil. Switch		50	200		250		214		<1	<1%						75	12	Switch- ing		A				.0005	
CR ₁	SIN916B Sil. Switch			200		250		124		<1	<1%						75	12	"						.0005	
CR ₂	2340338-1 Voltage Reference Zener T. C.			175		400		400		24	6%								Voltage Refer- ence						.00127	
CR ₁	IN5290 Current Reg.		50	200		600		600		25	4.1 %								Current Regu- lator						.00059	

20FAILURE RATE SOURCE (See Column 23)
AATM 695
B
C
D

21NOTE: R is assumed the transient and peak power does not exceed the safe limit.

22TOTAL FAILURE RATE.00286%/1000 HRS.

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PARTS APPLICATION ANALYSIS

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(SEMICONDUCTORS)

PROJECT: LSG
ASSEMBLY: Board # 9 and #1

SUB ASSEMBLY: A/D Converter

DATE: 1/20/71

SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MAXIMUM RATED CURRENT (mA)	MAX. TEMP °C		AVG PWR DISSIPATION (mw)				POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY								
			AMBIENT T _A	JUNCTION T _J	CASE T _C	RATED AT				ACTUAL RATED 25°C (Ambor case)	ACTUAL T _A or T _C	V _{CEO} RATED	V _{CB} ACTUAL	V _{CEO} RATED	V _{CE} ACTUAL	RATED			ACTUAL	RATE (%/1000 HRS)	F A I L U R E (See below)	F A I L U R E (%/1000 HRS)	F A I L U R E (%/1000 HRS)	F A I L U R E (%/1000 HRS)	TOTAL FAILURE RATE (%/1000 HRS)		
						25°C		ACTUAL	AMBIENT T _A																	CASE T _C	ACTUAL
						A	C																				
CR ₁	SIN914 Silicon	50 M 60197	50	200		250		214		<1	<1%					75	12	Switch- ing		A						.0005	
CR ₂	SIN914 Silicon			200				214		<1	<1%					75	12	"									
VR ₂	IN4572A Voltage Ref. T.C.	Dick- son		175		250		250		24	9.6 %							Voltage Refer- ence								.0007	
CR ₃	IN5299 Current Reg.	MOT	50	200		600		600		36	6%							Current Regulator		A						.00059	
FAILURE RATE SOURCE (See Column 23) A ATM 605 C _____ B _____ D _____										NOTE: R is assumed the transient and peak power does not exceed the safe limit.										TOTAL FAILURE RATE .00229 %/1000 HRS.							

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PARTS APPLICATION ANALYSIS

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(SEMICONDUCTORS)

PROJECT: LSG

DATE: 1/20/71

ASSEMBLY: Board #3

SUB ASSEMBLY: Analog Output Buffers

SCHEMATIC NO:

(Semiconductors)

CKT SYM NO.	TYPE DESIGNATION, SEMICONDUCTOR, POLARITY	MANUFACTURER	MAX. TEMP °C			AVG PWR DISSIPATION (mw)				POWER RATIO		MAXIMUM VOLTAGES				DIODE PIV		CIRCUIT FUNCTION or APPLI- CATION	PART SPECIAL ENVIRON- MENT (Define)	FOR RELIABILITY USE ONLY										
			AMBI- ENT TA	JUNC- TION TJ	CASE HOT SPOT TC	RATED AT				ACTUAL RATED 25°C Amb. or case	ACTUAL RATED TA or TC	VCBO V	VCB V	VCEO V	VCE V	RATED V	ACTUAL V			RATE (%/1000 HRS)	SOUR- CE RATE (%/1000 HRS) (See below)	FACIL- ITATE R RATE (%/1000 HRS)	FACIL- ITATE R RATE (%/1000 HRS)	FACIL- ITATE R RATE (%/1000 HRS)	FACIL- ITATE R RATE (%/1000 HRS)	FACIL- ITATE R RATE (%/1000 HRS)	TOTAL FAILURE RATE (%/1000 HRS)			
						25°C		AMBI- ENT TA	CASE TC																			ACTUAL TA	ACTUAL TC	
						AMBI- ENT TA	CASE TC																							
CR ₁	SIN914 Sil. Switch	60197 50 M	50	200		250		214		<1						75	12	Switch- ing												.0005
VR ₁	IN4572 T.C. Zener	Dick- son		175		250		250		20	8%							Temp. Control Zener												.0021
CR ₂	IN5299 Current Reg.	MOT	50	200		600		600		33	5.5 %							Current Regulator												.00059
22 FAILURE RATE SOURCE (See Column 23) A ATM 605 C _____ B _____ D _____										23 NOTE: It is assumed the transient and peak power does not exceed the safe limit.										24 TOTAL FAILURE RATE .00319 %/1000 HRS.										

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PROJECT: LSG
ASSEMBLY: Board #3

SUB ASSEMBLY: Analog Mux

DATE: 1/20/71
SCHEMATIC NO:

(Semiconductors)

[illegible]

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PROJECT: LSG
ASSEMBLY: Board #8

SUB ASSEMBLY: Demodulator

DATE: 1/20/71
SCHEMATIC NO:

(Semiconductors)

[illegible]

92004

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PROJECT: USG
ASSEMBLY: Boards #8 & 10

Demo- INT-OSC
SUB ASSEMBLY: & PWR Converter

DATE: 2/5/71
SCHEMATIC NO: _____

(Inductors & Transformers)

[illegible]

ВХА 321А

PROJECT: LSG

ASSEMBLY : CKT BD No. 7

SUB ASSEMBLY: Free Modes Filter

DATE: 1/10/71

SCHEMATIC NO:

[illegible]

FD-321A

SCHEMATIC NO:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CIRCUIT SYMBOL NUMBER	TYPE DEREGULATION (MIL OR MFR) CONSTRUCTION	MANUFACTURER	RESISTANCE VALUE (OHMS)	TOLERANCE (%)	POWER RATING (WATTS)	OPERATING MAXIMUM POWER (WATTS)	POWER LIMIT ON EXHAUSTION (WATTS)	MAXIMUM DUTY CYCLE	BULK AIR TEMPERATURE °C	CIRCUIT FUNCTION OR APPLICATION	BASIC FAILURE RATE (S/1000 HRS) - AT SOURCE (SEE BELOW)	SPECIAL ENVIRONMENTAL (DEFINING)	FAILURE RATE MULTIPLIER	FINAL FAILURE RATE (S/1000 HRS)	TOTAL RESISTOR COUNT PER TYPE	TOTAL FAILURE RATE (S/1000 HRS)	
R8	ACR07G472JS	A. Bradley	4.7k	±5	1/4	4.7	2%	1	50		.022	A		.001		.000022	
R15	RCR07G103JS	A. Bradley	10k	±5	1/4	10.0	2.5%										
R16	RCR07G333JS	A. Bradley	33k	±5	1/4	8.25	3%										
R7	RCR07G24JS	A. Bradley	220k	±5	1/4	1.08	.2%										
R8	RCR07G475JS	A. Bradley	4.7m	±5	1/4	<1	<1%										
R5	RCR07G106JS	A. Bradley	10m	±5	1/4	<1	<1%										
R6	RNR55C4751FR	MEPCO	4.75k	±1	1/10	4.75	4.75%				.178					.00018	
R12	RNR55C1022FR	MEPCO	10.2k	±1	1/10	10.0	10%										
R13	RNR55C1022FR	MEPCO	10.2k	±1	1/10	10.0	10%										
R4	RNR55C2212FR	MEPCO	22.1k	±1	1/10	10.8	11%										
R11	RNR55C2212FR	MEPCO	22.1k	±1	1/10	10.8	11%										
R1	RNR55C2742JA	MEPCO	27AK	±1	1/10	10.3	10%										
R12	RNR55C4752JR	MEPCO	47.5k	±1	1/10	8.3	8.3%										
R2	RCR07G226JS	A. Bradley	22m	±5	1/4	<1	<1%				.022					.000022	
R3	RNR55C2233FR	MEPCO	221k	±1	1/10	4.5	4.5%				.178					.00018	

19

FAILURE RATE SOURCES (FOR COLUMN #14)

A. ATM 605 B. _____

C. _____ D. _____

20

CALCULATED MTBF _____ HRS

21

TOTAL FAILURE RATE .001594 S/1000 HRS

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PROJECT: LSG

SUB ASSEMBLY: Stabilized Oscillator

DATE: 1/10/71

SCHEMATIC NO:

[illegible]

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[illegible]

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[illegible]

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RESISTORS

PROJECT: LSG

ASSEMBLY: Board #4

SUB ASSEMBLY: Tilt Servo Control

DATE: 1/10/71

SCHEMATIC NO:

(Resistors)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CIRCUIT SYMBOL NUMBER	TYPE DESIGNATION (MIL or MFR) AND CONSTRUCTION	MANUFACTURER	RESISTANCE VALUE (OHMS)	TOLERANCE (%)	POWER RATING (WATTS)	MAXIMUM OPERATING POWER (WATTS)	POWER RATIO OPERATING/ RATED	MAXIMUM DUTY CYCLE	BULK AIR TEMPERATURE °C	CIRCUIT FUNCTION OR APPLICATION	BASIC FAILURE RATE (S/1000 HRS) - AT SOURCE (SEE BELOW)	FOR USE OF RELIABILITY DEPT	SPECIAL ENVIRONMENTAL CONDITIONS	FAILURE RATE MULTIPLIER	FINAL FAILURE RATE (S/1000 HRS)	TOTAL RESISTOR COUNT PER TYPE	TOTAL FAILURE RATE (S/1000 HRS)
R5	RLR07C270G	Corning	27	±2%	1/4	2.4	1%	1	50		.022	A		.001			.000022
R10	RLR07C270G	Corning	27	±2%	1/4	2.4	1%										
R15	RLR07C270G	Corning	27	±2%	1/4	2.4	1%										
R20	RLR07C270G	Corning	27	±2%	1/4	2.4	1%										
R21	RCR07C102G	Corning	1k	±2%	1/4	5.0	2%										
R22	RCR07C102G	Corning	1k	±2%	1/4	5.0	2%										
R23	RCR07C102G	Corning	1k	±2%	1/4	5.0	2%										
R1	RCR07C242G	Corning	2.4k	±2%	1/4	6.5	3.8%										
R6	RCR07C242G	Corning	2.4k	±2%	1/4	6.5	3.8%										
R11	RCR07C242G	Corning	2.4k	±2%	1/4	6.5	3.8%										
R16	RCR07C242G	Corning	2.4k	±2%	1/4	6.5	3.8%										
R3	RCR07C512G	Corning	5.1k	±2%	1/4	1.5	<1%										
R8	RCR07C512G	Corning	5.1k	±2%	1/4	1.5											
R13	RCR07C512G	Corning	5.1k	±2%	1/4	1.5											
R18	RCR07C512G	Corning	5.1k	±2%	1/4	1.5											
R2	RCR07C103G	Corning	10k	±2%	1/4	1.0											
R4	RCR07C103G	Corning	10k	±2%	1/4	1.0											
R7	RCR07C103G	Corning	10k	±2%	1/4	1.0											
19						20						21					
FAILURE RATE SOURCES (FOR COLUMN #14)						CALCULATED MTBF _____ HRS						TOTAL FAILURE RATE .000396 %/1000 HRS					
A. ATM 605 _____ B. _____																	
C. _____ D. _____																	

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PROJECT:LSG

ASSEMBLY : Board #4

SUB ASSEMBLY: Tilt Servo Control

DATE: 1/10/71

SCHEMATIC NO:

(Resistors)

[illegible]

FORM 990

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(Resistors)

SCHEMATIC NO:

[illegible]

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PROJECT: LCS

ASSEMBLY: Board #3

SUB ASSEMBLY: Analog MUX

DATE: 1/10/71

SCHEMATIC NO:

[illegible]

FORM 9754

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RESISTORS

PROJECT: LGS

DATE: 1/10/71

ASSEMBLY: Board #3

SUB ASSEMBLY: Analog Output Buffers

SCHEMATIC NO:

(Resistors)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CIRCUIT SYMBOL NUMBER	TYPE DESIGNATION (MIL or MFR) CONSTRUCTION	MANUFACTURER	RESISTANCE VALUE (OHMS)	TOLERANCE (%)	POWER RATING (WATTS)	MAXIMUM OPERATING POWER (WATTS)	POWER RATIO ON RATING/BLT	MAXIMUM DUTY CYCLE	BULK AIR TEMPERATURE °C	CIRCUIT FUNCTION OR APPLICATION	BASIC FAILURE RATE (S/1000 HRS) - SEE BELOW	FOR USE OF RELIABILITY DEPT	SPECIAL ENVIRONMENTAL DESIGNS	FAILURE RATE MULTIPLIER	FINAL FAILURE RATE (S/1000 HRS)	TOTAL RESISTOR COUNT PER TYPE	TOTAL FAILURE RATE (S/1000 HRS)
R7	RLR05C243J	Corning	24k	±5	1/8	0.96	<1%	1	33		.275	A		.001			.00027
R8	TLR05C243J	Corning	24k	±5	1/8	0.96	<1%										
R9	RLR05C243J	Corning	24k	±5	1/8	0.96	<1%										
R10	RLR05C243J	Corning	24k	±5	1/8	0.96	<1%										
R16	RNR55C1002FR	MEPCO	10k	±1	1/10	2.5	2.5%				.178						.00018
R15	RNR55C4992FR	MEPCO	49.9k	±1	1/10	4.49	4.5%										
R23	RNR55C4992FR	MEPCO	49.9k	±1	1/10	4.49	4.5%										
R25	RNR55C1632D	MEPCO	16.5k	±.5	1/10	.48	1.5%										
R5	RNR55C2002D	MEPCO	20k	±.5	1/10	.25	1.2%										
R11	RNR55C2002D	MEPCO	20k	±.5	1/10	.25	1.2%										
R19	RNR55C2002D	MEPCO	20k	±.5	1/10	.25	1.2%										
R20	RNR55C2002D	MEPCO	20k	±.5	1/10	.25	1.2%										
R22	RNR55C2002D	MEPCO	20k	±.5	1/10	.25	1.2%										
R1	RNR55C1003F	MEPCO	100k	±1	1/10	.25	2.2%										
R2	RNR55C1003F	MEPCO	100k	±1	1/10	.25	2.2%										
R3	RNR55C1003F	MEPCO	100k	±1	1/10	.25	2.2%										
R4	RNR55C1003F	MEPCO	100k	±1	1/10	.25	2.2%										
19. FAILURE RATE SOURCES (FOR COLUMN #14)											20. CALCULATED MTBF _____ HRS		21. TOTAL FAILURE RATE: .00342 %/1000 HRS				
ATM 605 _____ B _____ C _____ D _____																	

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PROJECT: LGS

SUB ASSEMBLY: Analog Output Buffers

DATE: 1/10/71

SCHEMATIC NO:

[illegible]

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RESISTORS

PROJECT: LGS

ASSEMBLY: Board #1 & 9

SUB ASSEMBLY: A/D Converter

DATE: 1/10/71

SCHEMATIC NO:

(Resistors)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CIRCUIT SYMBOL NUMBER	TYPE DESIGNATION (MIL-STD-883C AND CONSTRUCTION)	MANUFACTURER	RESISTANCE VALUE (OHMS)	TOLERANCE (%)	POWER RATING (WATTS)	MAXIMUM OPERATING POWER (WATTS)	POWER RATIO OPERATING/ RATED	MAXIMUM DUTY CYCLE	BULK AIR TEMPERATURE °C	CIRCUIT FUNCTION OR APPLICATION	BASIC FAILURE RATE (%/1000 HRS) (SEE BELOW)	SPECIAL ENVIRONMENTS (DEFINITIONS)	FAILURE RATE MULTIPLIER	FINAL FAILURE RATE (%/1000 HRS)	TOTAL RESISTOR COUNT PER TYPE	TOTAL FAILURE RATE (%/1000 HRS)	
R1	RCR05G103JS	A. Bradley	10k	±1	1/8	2.5	5%	1	50		.022	A		.001		.00022	
R2					1/8	2.5	5%										
R3					1/8	2.5	5%										
R4					1/8	2.5	5%										
R5					1/8	2.5	5%										
R6					1/8	2.5	5%										
R7					1/8	2.5	5%										
R8					1/8	2.5	5%										
R9					1/8	2.5	5%										
R10					1/8	2.5	5%										
R32	RNR55C1002FS	MEPCO	10k	±1	1/10	2.5	2.5%				.178	A				.00018	
R33	RNR55C1002FS	MEPCO	10k	±1	1/10	2.5	2.5%				.178	A				.00018	
R34	S102	VISHAY	5k	±.01		5.0					1.78	B				.00178	
R29	S102	VISHAY	5k	±.1		5.0											
R21	S102	VISHAY	10k	±.05		2.5											
R24	S102	VISHAY	22k	±.05		1.16											
R22	S102	VISHAY	28.7k	±.05		1.04											
R28	S102	VISHAY	29.9k	±.05		1.19											
19 FAILURE RATE SOURCES (FOR COLUMN #14) A ATM 605 B Assumed C D											20 CALCULATED MTBF _____ HRS					21 TOTAL FAILURE RATE .01126 %/1000 HRS	

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RESISTORS

PROJECT: LSG

DATE: 1/10/71

ASSEMBLY: Board #1 & 9

SUB ASSEMBLY: A/D Converter

SCHEMATIC NO:

(Resistors)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CIRCUIT SYMBOL NUMBER	TYPE DESCRIPTION (MIL or MFR) CONSTRUCTION	MANUFACTURER	RESISTANCE VALUE (OHMS)	TOLERANCE (%)	POWER RATING (WATTS)	MAXIMUM OPERATING POWER (WATTS)	POWER RATIO OPERATING/ RATED	MAXIMUM DUTY CYCLE	BULK AIR TEMPERATURE °C	CIRCUIT FUNCTION OR APPLICATION	BASIC FAILURE RATE (1/1000 HRS) - AT SOURCE (USE BELOW)	FOR USE OF RELIABILITY DEPT	SPECIAL ENVIRONMENTS (OTHERS)	FAILURE RATE MULTIPLIER	FINAL FAILURE RATE (1/1000 HRS)	TOTAL FAILURE COUNT PER TYPE	TOTAL FAILURE RATE (1/1000 HRS)
R26	S102	VISHAY	30K	0.05	1.19		1	50			1.78	B		.001			.00178
R23	"	"	45K	"	0.54												
R25	"	"	50K	"	0.50												
R30	"	"	TBD	"													
R27	"	"	"	"													
R11	310737	"															
R12	"	"															
R13	"	"															
R14	"	"															
R15	"	"															
R16	"	"															
R17	"	"															
R18	"	"															
R19	"	"															
R20	"	"															
R31	S102	"	5.5K	0.05	4.45												
19										20		21					
FAILURE RATE SOURCES (FOR COLUMN #14)										CALCULATED MTBF _____ HRS		TOTAL FAILURE RATE .02848 1/1000 HRS					
A ATM 605 B Assures'																	
C _____ D _____																	

FORM 8871
BS-321A

PROJECT: LSG
ASSEMBLY: Board #15

DATE: 1/10/71
SCHEMATIC NO:

(Resistors)

[illegible]

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PROJECT: LSG

ASSEMBLY : Board #8

SUB ASSEMBLY: Integrator

DATE: 1/10/71

SCHEMATIC NO:

[illegible]

BS-321A

PARTS APPLICATION ANALYSIS

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RESISTORSPROJECT: LSG
ASSEMBLY: Board #7

SUB ASSEMBLY: Seismic Amp and Filter

DATE: 1/10/71
SCHEMATIC NO:

(Resistors)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18												
CIRCUIT SYMBOL NUMBER	TYPE DESCRIPTION (MIL-STD-883C) CONSTRUCTION	MANUFACTURER	RESISTANCE VALUE (OHMS)	TOLERANCE (%)	POWER RATING (WATTS)	MAXIMUM OPERATING POWER (WATTS)	POWER RATIO OPERATING RATED	MAXIMUM DUTY CYCLE	BULB AIR TEMPERATURE °C	CIRCUIT FUNCTION OR APPLICATION	BASIC FAILURE RATE (%/1000 HRS) - A - SOURCE (SEE BELOW)	FOR USE OF RELIABILITY DEPT	SPECIAL ENVIRONMENTS (DRAWING)	FAILURE RATE MULTIPLIER	FINAL FAILURE RATE (%/1000 HRS)	TOTAL RESISTOR COUNT PER TYPE	TOTAL FAILURE RATE (%/1000 HRS)												
R13	TBD													.001		.00018													
R14	"															.00018													
R10	RNR55E1211F	MEPCO	1.21K	±1	1/10	3.0	3.0%	1	50		.178	A				.00018													
R16	RNR55E4991F	"	4.99K	"	1/10	.090	<1%																						
R4	RNR55E1002F	"	10K	"	1/10	2.5	2.5%																						
R17	"	"	"	"	"	2.5	2.5%																						
R2	RNR55E6812F	"	6.81K	"	"	2.0	2%																						
R1	RNR55E5762F	Allen Bradley	57.6K	"	"	1.8	1.8%																						
R15	RCR07G473JS	Allen Bradley	47K	±5	1/4	2.5	1%				.022					.000022													
R18	"	"	"	"	"	2.5	1%				.178					.00018													
R3	RNR55E137eF	"	137K	±1	1/10	2.25	2.25%																						
R11	RNR55E4990D	MEPCO	499	±0.5	1/10	4.49	4.49%																						
R12	"	"	"	"	"	4.49	4.49%																						
R5	RNR55E5230F	"	523	±1	"	4.0	4%																						
R9	RNR55E1213F	"	121K	"	"	2.25	2.25%																						
R6	MDC	IRC	1M	±1	1/4	2.5	1%									.00018													
R7	"	"	2M	"	1/4	2.5										.00018													
R8	"	"	2M	"	1/4	2.5										.00018													
19										20										21									
FAILURE RATE SOURCES (FOR COLUMN #14)										CALCULATED MTBF _____ HRS										TOTAL FAILURE RATE .003082 %/1000 HRS									
A. ATM 605 B. _____																													
C. _____ D. _____																													

BS-321A

(Resistor)

DATE: 1/10/71
SCHEMATIC NO:

[illegible]

7188 1021

BS-321A

RESISTORS

PROJECT: LSG

DATE: 1/10/71

ASSEMBLY: Board #6

SUB ASSEMBLY: Mass Changing Servo

SCHEMATIC NO:

(Resistors)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CIRCUIT SYMBOL NUMBER	TYPE DESIGNATION (MIL OR MFR) CONSTRUCTION	MANUFACTURER	RESISTANCE VALUE (OHMS)	TOLERANCE	POWER RATING (WATTS)	MAXIMUM OPERATING POWER (WATTS)	POWER RATIO CORRECTION FACTOR	MAXIMUM DUTY CYCLE	BULK AIR TEMPERATURE °C	CIRCUIT FUNCTION OR APPLICATION	BASIC FAILURE RATE (x1000 HRS) - 25°C SOURCE (SEE BELOW)	FOR USE OF RELIABILITY DEPT	SPECIAL ENVIRONMENTS (OTHERS)	FAILURE RATE MULTIPLIER	FINAL FAILURE RATE (x1000 HRS)	TOTAL RESISTOR COUNT PER TYPE	TOTAL FAILURE RATE (x1000 HRS)
R24	RLR20C470G	Corning	47	±2	1/2	.012	< 1%	1	50		.275	A		.001			.00027
R25	"	"	"	"	"	.012	< 1%										
R18	RLR20C202G	"	2K	"	"	5.0	1%										
R19	"	"	"	"	"	5.0	1%										
R22	"	"	"	"	"	5.0	1%										
R23	"	"	"	"	"	5.0	1%										
R15	RNR55E1002FR	MEPCO	10K±1	1/10	2.5	.5%					.178						.00018
R11	RNR55E1372F	"	13.7K	"	"	2.5	.5%										
R5	RNR55E7872F	"	78.7K	"	"	1.5	< 1%										
R1	RLR07C102G	Corning	1K	±2	1/4	9.0	4%				.275						.00027
R12	"	"	"	"	"	9.0	4%										
R26	"	"	"	"	"	9.0	4%										
R27	"	"	"	"	"	9.0	4%										
R2	RLR076202G	"	2K	"	"	7.0	3%										
R6	"	"	"	"	"	7.0	3%										
R9	"	"	"	"	"	7.0	3%										
R14	"	"	"	"	"	7.0	3%										
19																	
20																	
21																	
FAILURE RATE SOURCES (FOR COLUMN #19)																	
A ATM 605 B _____																	
C _____ D _____																	
CALCULATED MTBF _____ HRS																	
TOTAL FAILURE RATE .00432 x1000 HRS																	

BS-321A

PROJECT: LSG DATE: 1/10/71
ASSEMBLY: Board #6 SUB ASSEMBLY: Mass Changing Servo SCHEMATIC NO: _____

FORM 991
BS-321A

(Resistors)

DATE: 1/10/71
SCHEMATIC NO: _____

[illegible]

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(Resistors)

SCHEMATIC NO:

1011 9384

ATM-979
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RESISTORS

PROJECT: LSG
ASSEMBLY: Board #15SUB ASSEMBLY: Instrument Housing
Temperature ControlDATE: 1/10/70
SCHEMATIC NO:

(Resistors)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CIRCUIT SYMBOL NUMBER	TYPE DESIGNATION (MIL & MFR) CONSTRUCTION	MANUFACTURER	RESISTANCE VALUE (OHMS)	TOLERANCE (%)	POWER RATING (WATTS)	MAXIMUM OPERATING POWER (WATTS)	POWER RATIO OPERATING/ RATED	MAXIMUM DUTY CYCLE	BULK AIR TEMPERATURE °C	CIRCUIT FUNCTION OR APPLICATION	BASIC FAILURE RATE (%/1000 HRS) - 21 - SOURCE (SEE BELOW)	FOR USE OF RELIABILITY DEPT	SPECIAL ENVIRONMENTS (DESIGNS)	FAILURE RATE MULTIPLIER	FINAL FAILURE RATE (%/1000 HRS)	TOTAL FAILURE COUNT PER TYPE	TOTAL FAILURE RATE (%/1000 HRS)
R1	RLR07C100G	Corning	10	±2	1/4	2.4	1%	1	50		.275	A		.001			.00027
R2	"	"	"	"	"	2.4	1%				.275						.00027
R3	TBD	MEPCO	221K	±1	1/10	2.2	2.2%				.275						.00027
R4	RND55E2552F	"															
R5	TBD	"															
R8	RNR55E1003F	"	100K	±1	1/10	.25	< 1%				.178						.00018
R9	"	"	"	"	"	.25	< 1%				.178						.00018
R10	TBD	"															.00027
R13	RNR65E1004FR	"	1M	±1	1/4	< 1	< 1%				.178						.00018
R15	"	"	"	"	1/4	< 1	< 1%				.178						.00018
R14	RLR07C273GB	"	27K	±2	1/4	.69	< 1%										
R16	RLR07C104GR	"	100K	±2	1/4	< 1	< 1%										
R17	RLR076682GR	"	68K	"	1/4	4.35	1.5%										
R26	"	"	"	"	1/4	4.35	1.5%										
R18	RLR07C512GR	"	5.1K	"	1/4	4.9	2%										
R19	RLR07C333GR	"	33K	"	1/4	< 1	1%										
R20	"	"	"	"	1/4	< 1	1%										
19											20				21		
FAILURE RATE SOURCES (FOR COLUMN #14)											CALCULATED MTBF _____ HRS				TOTAL FAILURE RATE: .00423 %/1000 HRS		
A ATM 605 B _____																	
C _____ D _____																	

FORM 224
BS-321A

(Resistors)

SCHEMATIC NO:

FOIA b 7(D)

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(Resistor)

SCHEMATIC NO:

1994

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(Resistors)

ASSEMBLY: Board #8

DATE: 1/10/71

SCHEMATIC NO:

FORM 950i

ATM-979
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(MICROCIRCUITS)

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SCHEMATIC NO:

[illegible]

BxA 679

PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG

DATE: 1/15/71

ASSEMBLY: Board #7

SUB ASSEMBLY: Seismic Ampl & Filter

SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU FACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY			
				AMBI- ENT	JUN- TION	JUN- TION	DEGRAD- ATION	ACTU- AL	DEGRAD- ATION	FAN IN %	% OF MAX I OR V	FAN OUT %	LOAD- ING				RATE (%/1000 HRS)	SOURCE	FULL RATED	TOTAL FAILURE RATE (%/1000 HRS)
A1	Op. Ampl. LM108AH/883	Nat. Semi.	Lin- ear	50	125	60	±20	±10	±2			60				Op. Ampl.	A			.0020
A3	Op. Ampl. LM108AH/883	Nat. Semi.	Lin- ear	50	125	60	±20	±10	±2			60				Op. Ampl.	A			.0020
A2	Op. Ampl. 1402-02	Phil- brick	Lin- ear	50	85	55	±24	±10	±4			70				Op. Ampl.	A			.0064
23 FAILURE RATE SOURCE (See Column 19) A <u>ATM 605A</u> C _____ B _____ D _____				24 NOTE: DERATED VOLTAGE IS DETERMINED BY: $V_{MAX} = V_{NOM} + .5 (V_{RATED MAX} - V_{NOM})$ $V_{MIN} = V_{NOM} - .5 (V_{NOM} - V_{RATED MIN})$										25 TOTAL FAILURE RATE <u>.0104</u> %/1000 HRS						

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG
ASSEMBLY: Board #6

SUB ASSEMBLY: Mass Change Servo

DATE: 1/15/71

SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	M A N U F A C T U R E R	T Y P E	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY			
				A M B I E N T	J U N C T I O N	A J U N C T I O N	D M A X I M U M	A C T U A L	D M I N I M U M	FAN I N %	% OF MAX I/O R V	FAN O U T %	L O A D I N G %				R A T E (%/1000 HRS)	S O U R C E	F A U L T R A T E P E R T Y P E	T O T A L F A I L U R E R A T E (%/1000 HRS)
11	LPT2L Gate SNA54L00	TI	Logic	50	125	60	5.3	5	4.7			50				Gate		A		.0020
12	LPT2L F.F. SNA54L78	TI	Logic	50	125	60	5.3	5	4.7			70				Flip Flop		A		.0020
13	LPT2L F.F. SNA54L78	TI	Logic	50	125	60	5.3	5	4.7			70				Flip Flop		A		.0020
25 FAILURE RATE SOURCE (See Column 19) A <u>ATM 605A</u> C _____ B _____ D _____				26 NOTE: DERATED VOLTAGE IS DETERMINED BY: $V_{MAX} = V_{NOM} + .5 (V_{RATED} - V_{NOM})$ $V_{MIN} = V_{NOM} - .5 (V_{NOM} - V_{RATED MIN})$										27 TOTAL FAILURE RATE <u>.0060</u> %/1000 HRS						

8xA 679

PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG
ASSEMBLY: Board #4 & 5

SUB ASSEMBLY: Screw Servo

DATE: 1/15/71

SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU- FACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED	CLOCK WIDTH	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY				
				AMBI- ENT	JUNC- TION	JUNC- TION	MAX RATED	ACTU- AL	MIN RATED	FAN IN %	% OF MAX I/O R V	FAN OUT %	LOAD %	% OF MAX	MIN ACTUAL %		RATE (%/1000 HRS)	SOURCE	FULL RIPPLE VOLTAGE	TOTAL FAILURE RATE PER TYPE	TOTAL FAILURE RATE (%/1000 HRS)
	LPT2L Gate SNA54L00	TI	Logic	50	125	60	5.30	5.0	4.7			50				Gate		A		.0080	
	LPT2L Gate SNA54L10	TI	Logic	50	125	60	5.30	5.0	4.7			60				Gate		A		.0040	
	LPT2L Gate SNA54L20	TI	Logic	50	125	60	5.30	5.0	4.7			60				Gate		A		.0020	
	LPT2L Gate SNA54L51	TI	Logic	50	125	60	5.30	5.0	4.7			50				Gate		A		.0020	
	LPT2L F.F. SNA54L72	TI	Logic	50	125	60	5.30	5.0	4.7			70				Flip Flop		A		.0020	
	LPT2L F.F. SNA54L78	TI	Logic	50	125	60	5.30	5.0	4.7			60				Flip Flop		A		.0020	
	LPT2L Contr. SNA54L93	TI	Logic	50	125	60	5.30	5.0	4.7			50				Counter		A		.0080	
	S8J80J	Sig- netics	Logic	50	125	60	6.0					60				Nand Interface Gate		A		.0020	
23 FAILURE RATE SOURCE (See Column 18) A <u>ATM 605A</u> C _____ B _____ D _____							24 NOTE: DERATED VOLTAGE IS DETERMINED BY: $V_{MAX} = V_{NOM} + .5 (V_{RATED MAX} - V_{NOM})$ $V_{MIN} = V_{NOM} - .5 (V_{NOM} - V_{RATED MIN})$							25 TOTAL FAILURE RATE <u>.0240</u> %/1000 HRS							

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG

DATE: 1/15/71

ASSEMBLY: Board #10

SUB ASSEMBLY: Shaft Encoder Elect.

SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU FACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY				
				A C T U A L	J U N C T I O N	A C T U A L	D E R A T E D	A C T U A L	D E R A T E D	FAN IN %	% OF MAX I OR V	FAN OUT %	L O A D I N G				RATE (%/1000 HRS)	S O U R C E	F A U L T R A P P E R	T O O T A L P E R T Y P E	TOTAL FAILURE RATE (%/1000 HRS)
127	T2L Inv. SNA54L04	TI	Dig	50	125	60	5.3	5	4.7			50				Inverter		A			.0080
thru 131	T2L Inv. SNA54L04	TI		50	125		5.3	5	4.7			60				Inverter		A			
126	T2L JK F.F. SNA54L73	TI		50	125		5.3	5	4.7			70				J-K Flip Flop		A		.0020	
125	T2L Gate SNA54L20	TI		50	125		5.3	5	4.7			60				Gate		A		.0020	
16	T2L Gate SNA54L10	TI		50	125		5.3	5	4.7			60				Gate		A		.0360	
thru 124	T2L Gate SNA54L10	TI		50	125		5.3	5	4.7			60				Gate		A			
11	T2L Gate SNA54L51	TI		50	125		5.3	5	4.7			60				Gate		A		.0080	
thru 15	T2L Gate SNA54L51	TI		50	125		5.3	5	4.7			60				Gate		A			
131	LPT2L F.F. SNA54L78	TI		50	125		5.3	5	4.7			60				Flip Flop		A		.0020	

22 FAILURE RATE SOURCE (See Column 19)

A ATM 605A C _____

B _____ D _____

23 NOTE: DERATED VOLTAGE IS DETERMINED BY:

$V_{MAX} = V_{NOM} + .5 (V_{RATED MAX} - V_{NOM})$

$V_{MIN} = V_{NOM} - .5 (V_{NOM} - V_{RATED MIN})$

24 TOTAL FAILURE RATE .0580 %/1000 HRS

BxA 679

PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG

ASSEMBLY: Board #15

SUB ASSEMBLY: Inst. Housing Temp. Control

DATE: 1/15/71

SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU FACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY			
				AC TUAL ENV T	JUN CTED ION	JUN CTU AL ION	DE X I TUM	AC TUAL	DE X I TUM	FAN IN %	% OF MAX I/O V	FAN OUT %	LO AD ING				RATE (%/1000 HRS)	SOURCE	FM ALT R PER TYPE	TOTAL FAILURE RATE (%/1000 HRS)
I3	Voltage Ref. LM103-5.1/883	Nat. Semi	Lin- ear	50	125	60	>5	5	4				70			Voltage Regulator	A			.0020
I4	Voltage Ref. LM103-5.1/883	Nat. Semi	Lin- ear	50	125	60	>5	5	4				70			Voltage Regulator	A		.0020	
I7	Voltage Ref. LM103-5.1/883	Nat. Semi	Lin- ear	50	125	60	>5	5	4				60			Voltage Regulator	A		.0020	
I1	Voltage Regul. SM105 G	Nat. Semi	Lin- ear	50	150	60	50	20	8.5				60			Voltage Regulator	A		.0020	
I2	Voltage Regul. SM105 G	Nat. Semi	Lin- ear	50	150	60	50	20	8.5				60			Voltage Regulator	A		.0020	
A1	Op. Ampl. NH0001AH/883	Nat. Semi	Lin- ear	50	125	60	≤±20	10	±5≤				70			Op. Amplifier	A		.0020	
A2	Op. Ampl. NH0001AH/883	Nat. Semi	Lin- ear	50	125	60	≤±20	10	±5≤				70			Op. Amplifier	A		.0020	
I10	Voltage Ref. LM103-2.4/883	Nat. Semi	Lin- ear	50	125	60	>5	5	4				60			Voltage Reference	A		.0020	
I11	Voltage Ref. LM103-2.4/883	Nat. Semi	Lin- ear	50	125	60	>5	5	4				60			Voltage Reference	A		.0020	

79 FAILURE RATE SOURCE (See Column 19)

A ATM 605A C _____

B _____ D _____

20 NOTE: DERATED VOLTAGE IS DETERMINED BY:
 $V_{MAX} = V_{NOM} + .5 (V_{RATED MAX} - V_{NOM})$
 $V_{MIN} = V_{NOM} - .5 (V_{NOM} - V_{RATED MIN})$

20 TOTAL FAILURE RATE .0180 %/1000 HRS

8xA 679

PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG

DATE: 1/15/71

ASSEMBLY: Board #1

SUB ASSEMBLY: Digital MUX

SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU FACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY			
				A C T U A L	J U N C T I O N	A C T U A L	D E R A T E D M A X	A C T U A L	D E R A T E D M A X	FAN IN %	% OF MAX I OR V	FAN OUT %	L O A D I N G %				RATE (%/1000 HRS)	SOURCE N	F A U L T R A P P E R	T O T A L P E R T Y P E
I1	Shift Register SNA54L95	TI	Logic	50	125	60	5.3	5.0	4.7			50				Register		A		.0020
I2	Shift Register SNA54L95	TI	Logic	50	125	60	5.3	5.0	4.7			60				Register		A	.0020	
I3	Shift Register SNA54L95	TI	Logic	50	125	60	5.3	5.0	4.7			50				Register		A	.0020	
I4	T2L Gate SNA54L54	TI	Logic	50	125	60	5.3	5.0	4.7			50				Gate		A	.0180	
thru I13	T2L Gate SNA54L54	TI	Logic	50	125	60	5.3	5.0	4.7			50				Gate		A		
<small>23</small> FAILURE RATE SOURCE (See Column 19) A <u>ATM 605A</u> C _____ B _____ D _____							<small>24</small> NOTE: DERATED VOLTAGE IS DETERMINED BY: $V_{MAX} = V_{NOM} + .5 (V_{RATED MAX} - V_{NOM})$ $V_{MIN} = V_{NOM} - .5 (V_{NOM} - V_{RATED MIN})$							<small>25</small> TOTAL FAILURE RATE <u>.0240</u> %/1000 HRS						

8xA 679

PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG

DATE: 1/15/71

ASSEMBLY: Board #1

SUB ASSEMBLY: Digital MUX Control

SCHEMATIC NO:

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU- FACTURER	T Y P E	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY			
				AM- BIEN- T	JUN- TION	ACTU- TION	MAX EX- TREMUM	ACTU- AL	MIN EX- TREMUM	FAN IN %	% OF MAX FOR V	FAN OUT %	LOA- DING %				RATE (%/1000 HRS)	SOURCE	FM FAULT RATE	TC TOTAL PER TYPE
I5	T2L Gate SN54L00	TI	Logic	50	125	60	5.3	5	4.7			60				Gate	A			.0020
I4	INV T2L SN54L04	TI	Logic	50	125	60	5.3	5	4.7			60				Inverter	A		.0020	
I6	INV T2L SN54L04	TI	Logic	50	125	60	5.3	5	4.7			60				Inverter	A		.0020	
I3	T2L Gate SN54L10	TI	Logic	50	125	60	5.3	5	4.7			60				Gate	A		.0020	
I2	T2L Gate SN54L20	TI	Logic	50	125	60	5.3	5	4.7			60				Gate	A		.0020	
I1	SN54L93	TI	Logic	50	125	60	5.3	5	4.7			60				Gate	A		.0020	

23 FAILURE RATE SOURCE (See Column 19)

A ATM 605A C

B D

24 NOTE: DERATED VOLTAGE IS DETERMINED BY:
 $V_{MAX} = V_{NOM} + .8 (V_{RATED MAX} - V_{NOM})$
 $V_{MIN} = V_{NOM} - .8 (V_{NOM} - V_{RATED MIN})$

25 TOTAL FAILURE RATE .0120 %/1000 HRS

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG
ASSEMBLY: Board #2

SUB ASSEMBLY: Command Decoder & Drives

DATE: 1/15/71

SCHEMATIC NO:

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	M A N U F A C T U R E R	T Y P E	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY				
				A M B I E N T	J U N C T I O N	J U N C T I O N	D E R A T E D M A X I M U M	A C T U A L	D E R A T E D M A X I M U M	FAN IN %	% OF MAX I/O R V	FAN OUT %	L O A D I N G %				RATE (%/1000 HRS)	S C R E W S	F A I L U R E R A T E	T O O T A L F A I L U R E R A T E P E R T Y P E	TOTAL FAILURE RATE (%/1000 HRS)
11	T2L Hex Driver S8T90J	Sig- netics	Logic	50	125	60	6					50				Hex Inverter Interface		A			.0020
12	T2L Hex Driver S8T90J	Sig- netics	Logic	50	125	60						50				Hex Inverter Interface		A			.0020
13	T2L INV SNA54L04	TI	Logic	50	125	60	5.3	5.0	4.7			60				Inverter Interface		A			.0020
14	T2L INV SNA54L04	TI	Logic	50	125	60	5.3	5.0	4.7			60				Inverter Interface		A			.0020
15	T2L Decoder UAM93L1151X	Fair- child	Logic	50	125	60	7.0	3.5	0.5			60				Decoder		A			.0020
FAILURE RATE SOURCE (See Column 19) A ATM 605A C _____ B _____ D _____							NOTE: DERATED VOLTAGE IS DETERMINED BY: $V_{MAX} = V_{NOM} + .5 (V_{RATED MAX} - V_{NOM})$ $V_{MIN} = V_{NOM} - .5 (V_{NOM} - V_{RATED MIN})$							TOTAL FAILURE RATE .0100 %/1000 HRS							

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG

DATE: 1/15/71

ASSEMBLY: Board #2

SUB ASSEMBLY: Command Counter

SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANUFACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY				
				AC TUE L	R J U N C T I O N	A C T U A L	D E A R T H E M	A C T U A L	D E R I V E D	FAN IN %	% OF MAX I OR V	FAN OUT %	L O A D I N G				RATE (%/1000 HRS)	SOURCE	F M U L T I P L I C A T I O N	T O T A L F A I L U R E R A T E (%/1000 HRS)	
11	T2L SNA54L86	TI	Logic	50	125	60	5.3	5	4.7			50				Flip Flop	A			.0020	
12	T2L F.F. SNA54L78	TI	Logic	50	125	60	5.3	5	4.7			60				Flip Flop	A		.0020		
13	T2L F.F. SNA54L78	TI	Logic	50	125	60	5.3	5	4.7			60				Flip Flop	A		.0020		
14	T2L F.F. SNA54LT2	TI	Logic	50	125	60	5.3	5	4.7			60				Flip Flop	A		.0020		
15	T2L Gate SNA54L00	TI	Logic	50	125	60	5.3	5	4.7			60				Gate	A		.0020		
16	T2L Gate SNA54L00	TI	Logic	50	125	60	5.3	5	4.7			60				Gate	A		.0020		
17	T2L Gate SNA54L00	TI	Logic	50	125	60	5.3	5	4.7			60				Gate	A		.0020		

23 FAILURE RATE SOURCE (See Column 19)

A ATM 605A C _____

B _____ D _____

24 NOTE: DERATED VOLTAGE IS DETERMINED BY:

$V_{MAX} = V_{NOM} + .5(V_{RATED MAX} - V_{NOM})$

$V_{MIN} = V_{NOM} - .5(V_{NOM} - V_{RATED MIN})$

25 TOTAL FAILURE RATE .0140 %/1000 HRS

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG

DATE: 1/15/71

ASSEMBLY: Board #7

SUB ASSEMBLY: Free Modes Filter

SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU- FACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED	CLOCK WIDTH	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY			
				AMBI- ENT ACTU- AL	JUN- TION RATED	JUN- TION ACTU- AL	MAXI- MUM DEXT- REM	ACTU- AL	MINI- MUM DEXT- REM	FAN IN %	% OF MAX I OR V	FAN OUT %	LO- AD %	% OF MAX	MIN ACTUAL %		RATE (%/1000 HRS)	SOURCE	FAULT RPL- IER	TC DU- ANT PER TYPE
A1	Op. Ampl. 1402-02	Phil- brick	Lin- ear	50	85	55	±24	±10	±4				70			Oper- ational Amplifier	A			.0064
23 FAILURE RATE SOURCE (See Column 18)				24 NOTE: DERATED VOLTAGE IS DETERMINED BY: $V_{MAX} = V_{NOM} + .5 (V_{RATED MAX} - V_{NOM})$ $V_{MIN} = V_{NOM} - .5 (V_{NOM} - V_{RATED MIN})$										25 TOTAL FAILURE RATE <u>.0064</u> %/1000 HRS						
A <u>ATM 605A</u> C _____ B _____ D _____																				

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG
ASSEMBLY: Board #8

SUB ASSEMBLY: Post-Ampl.

DATE: 1/15/71

SCHEMATIC NO:

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANUFACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY				
				A C M B I E N T	J U N C T I O N	A C T U A L	M A X I M U M D E R A T E D	A C T U A L	M I N I M U M D E R A T E D	FAN I N %	% OF MAX I O R V	FAN O U T %	L O A D I N G %				RATE (%/1000 HRS)	SOURCE Gen Source	F A U L T R A T I N G	T O O T A L P E R T Y P E	TOTAL FAILURE RATE (%/1000 HRS)
A ₁	Op. Ampl. SM101G-1	85M0 3910	Lin- ear	50	85	55	±24	±10	±4				70			Op. Amplifier		A			.0064
VR ₁	Voltage Reg. LM103-5.1	Nat. Sem.	Lin- ear	50	125	60	>5	5	4				70			Voltage Regulator		A			.0080
UR ₄	Voltage Reg. LM103-5.1	Nat. Sem.	Lin- ear	50	125	60	>5	5	4				60			Voltage Regulator		A			.0080
I ₄	Analog Gate CDA2-3	Crys- talonic	Lin- ear	50												Analog Gate		A			.0064
I ₅	Analog Gate CDA2-3	Crys- talonic	Lin- ear	50												Analog Gate		A			.0064
I ₁	LP/T ² L Gate SNA54L 30	TI	Log- ic	50	125	60	5.3	5	4.7				50			Gate		A			.0020
I ₂	LP/T ² L F.F SNA54L78	TI	Log- ic	50	125	60	5.3	5	4.7				50			Flip Flop		A			.0020
I ₃	LP/T ² L F.F SNA54 78	TI	Log- ic	50	125	60	5.3	5	4.7				50			Flip Flop		A			.0020
FAILURE RATE SOURCE (See Column 19)				NOTE: DERATED VOLTAGE IS DETERMINED BY: V _{MAX} = V _{NOM} + .5 (V _{RATED MAX} - V _{NOM}) V _{MIN} = V _{NOM} - .5 (V _{NOM} - V _{RATED MIN})										TOTAL FAILURE RATE .0412 %/1000 HRS							
A ATM 605A																					
B																					
C																					
D																					

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PROJECT: LSG
ASSEMBLY: Board #4

SUB ASSEMBLY: Tilt Servo

DATE: 1/15/71

SCHEMATIC NO: .

[illegible]

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG

DATE: 1/15/71

ASSEMBLY: Board #4

SUB ASSEMBLY: Tilt Servo

SCHEMATIC NO:

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANUFACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED	CLOCK WIDTH	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY			
				AMBI- ENT	JUNC- TION	CON- DUCTION	DE- RATED	ACTU- AL	DE- RATED	FAN IN %	% OF MAX IOV	FAN OUT %	LO- ADING	% OF MAX	MIN ACTUAL %		RATE (%/1000 HRS)	SOURCE	FAULT RATES	TC DO TAN CT
I ₁	LPT ² L Gate SNA54L00	TI	Log- ic	50	125	60	5.3	5	4.7			60				Gate		A		.0020
I ₄	LPT ² L Gate SNA54L00	TI	Log- ic	50	125	60	5.3	5	4.7			60				Gate		A	.0020	
I ₆	LPT ² L Gate SNA54L00	TI	Log- ic	50	125	60	5.3	5	4.7			60				Gate		A	.0020	
I ₇	LPT ² L Gate SNA54L00	TI	Log- ic	50	125	60	5.3	5	4.7			60				Gate		A	.0020	
I ₉	LPT ² L Gate SNA54L00	TI	Log- ic	50	125	60	5.3	5	4.7			60				Gate		A	.0020	
I ₁₀	LPT ² L Gate SNA54L00	TI	Log- ic	50	125	60	5.3	5	4.7			60				Gate		A	.0020	
I ₃	LPT ² L F. F. SNA54L72	TI	Log- ic	50	125	60	5.3	5	4.7			50				Flip Flop		A	.0020	
I ₅	LPT ² L F. F. SNA54L78	TI	Log- ic	50	125	60	5.3	5	4.7			50				Flip Flop		A	.0020	
I ₂	LPT ² L Control SN54L93	TI	Log- ic	50	125	60	5.3	5	4.7			50				Controller		A	.0020	

19 FAILURE RATE SOURCE (See Column 19)

A ATM 605 A C

B D

20 NOTE: DERATED VOLTAGE IS DETERMINED BY:
 $V_{MAX} = V_{NOM} \cdot .5 (V_{RATED} \cdot V_{NOM})$
 $V_{MIN} = V_{NOM} \cdot .5 (V_{NOM} \cdot V_{RATED} \cdot MIN)$

21 TOTAL FAILURE RATE .0180 %/1000 HRS

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG

DATE: 1/15/71

ASSEMBLY: Board #15

SUB ASSEMBLY: Temp. Monitor

SCHEMATIC NO:

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU FACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY			
				AM BUI ENT	JUN TION	JUN TION	DE X I TUM	ACT UAL	DE X I TUM	FAN IN %	% OF MAX I OR V	FAN OUT %	LO AD ING				RATE (%/ 1000 HRS)	SOUR CE	F A L T R A T E	T O T A L F A I L U R E R A T E (%/1000 HRS)
A ₁	Op. Amp. NH0001AH/883	Nat. Semi	Linear	50	125	60	<+20	10	+5<				70			Op. Amp	A			.0020
I ₅	Volt Reference LMID3-4.3/883	"	"	50	125	60	>5	5	4				60			Voltage Ref.	A			.0020
I ₆	Volt Reference LMID3-4.3/883	"	"	50	125	60	>5	5	4				60			Voltage Ref.	A			.0020
23 FAILURE RATE SOURCE (See Column 19) A ATM 605A C B D				24 NOTE: DERATED VOLTAGE IS DETERMINED BY: V _{MAX} = V _{NOM} + .5 (V _{RATED MAX} - V _{NOM}) V _{MIN} = V _{NOM} - .5 (V _{NOM} - V _{RATED MIN})											25 TOTAL FAILURE RATE .0060 %/1000 HRS					

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG

DATE: 1/15/71

ASSEMBLY: Board #2

SUB ASSEMBLY: Dig

SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU FACTURER	T YPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY				
				A C M B I E N T	J U N C T I O N	J U N C T I O N	D E R A T E D M A X I M U M	A C T U A L	D E R A T E D M I N I M U M	FAN IN %	% OF MAX I OR V	FAN OUT %	L O A D %				RATE (%/1000 HRS)	S O U R C E	F A U L T R A T E P E R T Y P E	T O T A L F A I L U R E R A T E (%/1000 HRS)	
I ₅	S8T90J	Sig- netics	Dig	50	125	60	6.0					70				Hex inver ter Inter- face		A			.0020
I ₁	SNA54L04	TI	Dig	50	125	60	5.3	5	4.7			60				Hex inver ter Inter- face		A			.0020
I ₂	SNA54L04	TI	Dig	50	125	60	5.3	5	4.7			60				Hex inver ter Inter- face		A			.0020
I ₃	SNA54L04	TI	Dig	50	125	60	5.3	5	4.7			60				Hex inver ter Inter- face		A			.0020
I ₄	SNA54L04	TI	Dig	50	125	60	5.3	5	4.7			60				Hex inver ter Inter- face		A			.0020
<small>23</small> FAILURE RATE SOURCE (See Column 19) A <u>ATM 605A</u> C _____ B _____ D _____				<small>24</small> NOTE: DERATED VOLTAGE IS DETERMINED BY: $V_{MAX} = V_{NOM} + .5(V_{RATED MAX} - V_{NOM})$ $V_{MIN} = V_{NOM} - .5(V_{NOM} - V_{RATED MIN})$										<small>25</small> TOTAL FAILURE RATE <u>.0100</u> %/1000 HRS							

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG
ASSEMBLY: Board # 1 & 9

SUB ASSEMBLY: A
H/D Converters

DATE: 1/15/71
SCHEMATIC NO:

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU- FACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED	CLOCK WIDTH	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY				
				A M B I E N T	J U N C T I O N	J U N C T I O N	D E R A T E D	A C T U A L	D E R A T E D	FAN IN %	% OF MAX I/O R/V	FAN OUT %	L O A D %	% OF MAX	MIN ACTUAL %		RATE (%/1000 HRS)	S U R C E	F U L L R A T E D T Y P E	T O T A L F A I L U R E R A T E (%/1000 HRS)	
I ₁	T ² L F.F. SNA54L73	TI	Log	50	125	60	5.3	5	4.7			50				Flip Flop		A			.0100
thru I ₅	T ² L F.F. SNA54L73	TI	Log	50	125	60	5.3	5	4.7			60				Flip Flop		A			
I ₆	T ² L Gate SNA54L00	TI	Log	50	125	60	5.3	5	4.7			60				Gate		A			.0100
thru I ₁₁	T ² L Gate SNA54L00	TI	Log	50	125	60	5.3	5	4.7			60				Gate		A			
I ₁₂	Analog Switch CDA2-1	Crys- talonic	Linear	50									70					A			.0064
thru I ₁₆	Analog Switch CDA2-1	Crys- talonic	Linear	50									70					A			.0064
A ₁	Op. Amp. NH0001AH/883	Nat Semi	Linear	50	125	60	<+20	10	+5<				60			Op. Amp		A			.0100
thru A ₅	Op. Amp. NH0001AH/883	Nat Semi	Linear	50	125	60	<+20	10	+5<				60			Op. Amp		A			
thru D ₅	Voltage Reg. LM103-5.1/883	Nat Semi	Linear	50	125	60	>5	5	4				60			Voltage Reg.		A			.0020
FAILURE RATE SOURCE (See Column 19) A ATM 605A B _____ C _____ D _____				NOTE: DERATED VOLTAGE IS DETERMINED BY: V _{MAX} = V _{NOM} + .5 (V _{RATED MAX} - V _{NOM}) V _{MIN} = V _{NOM} - .5 (V _{NOM} - V _{RATED MIN})										TOTAL FAILURE RATE .0448 %/1000 HRS .0664							

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSG
ASSEMBLY: Board #3

SUB ASSEMBLY: Analog Output Buffer

DATE: 1/15/71

SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	M A N U F A C T U R E R	T Y P E	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED	CLOCK WIDTH	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY			
				A M B I E N T	J U N C T I O N	J U N C T I O N	D M A X I M U M	A C T U A L	M I N I M U M	FAN IN %	% OF MAX I OR V	FAN OUT %	L O A D %	% OF MAX	MIN ACTUAL %		RATE (%/1000 HRS)	S U B S T R A T E G Y	M U L T I P L I E R	T O T A L P E R T Y P E
I ₁	Op. Amp NH0001AH/883	Nat Semi	Linear	50	125	60	≤±20	±10	±5≤				70			Op. Amp.	A			.0140
thru I ₇	Op. Amp. NH0001AH/883	Nat Semi	Linear	50	125	60	≤±20	±10	±5≤				70			Op. Amp.	A		.0140	
<small>20</small> FAILURE RATE SOURCE (See Column 19) A <u>ATM 605A</u> C _____ B _____ D _____							<small>21</small> NOTE: DERATED VOLTAGE IS DETERMINED BY: $V_{MAX} = V_{NOM} + .5(V_{RATED MAX} - V_{NOM})$ $V_{MIN} = V_{NOM} - .5(V_{NOM} - V_{RATED MIN})$							<small>22</small> TOTAL FAILURE RATE <u>.0140</u> %/1000 HRS						

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PARTS APPLICATION ANALYSIS

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(MICROCIRCUITS)

PROJECT: LSC
ASSEMBLY: Board #3

SUB ASSEMBLY: Analog MUX

DATE: 1/15/71
SCHEMATIC NO: _____

(Microcircuits)

CKT SYM NO.	TYPE DESIGNATION	MANU- FACTURER	TYPE	MAX TEMP °C			VOLTAGES			INPUTS		OUTPUTS		SPEED % OF MAX	CLOCK WIDTH MIN ACTUAL %	CIRCUIT FUNCTION OR APPLI- CATION	FOR RELIABILITY USE ONLY			
				AM- BIEN- T	JUN- TION	JUN- TION	MA- XIM- UM	ACTU- AL	DE- TER- MIN- UM	FAN IN %	% OF MAX FOR V	FAN OUT %	LO- AD- ING				RATE (%/1000 HRS)	SOURCE	TC OUL- T	TOTAL FAILURE RATE (%/1000 HRS)
I ₃	T ² L Gate SNA54L00	TI	Log	50	125	60	5.3	5	4.7			70				Gate	A		.0020	
I ₄	T ² L Shift Right SNA54L95	TI	Log	50	125	60	5.3	5	4.7			60				Shift Register	A		.0020	
I ₅	T ² L Shift Right SNA54L95	TI	Log	50	125	60	5.3	5	4.7			60				Shift Register	A		.0020	
I ₆	Op. Amp. NH0001AH/883	Nat Semi	Linear	50	125	60	<±20	±10	±5<			70				Op. Amp	A		.0020	
I ₂	Translator VA1026	United Air- craft	Logic	50	125	60	5.3	5	4.7			50				Voltage Translator	A		.0020	
I ₁	Multiplex Gate MEM2009	Gen. Inst.	Logic	50	125	60	5.3	5	4.7			60				Multiplex Gate	A		.0020	

22 FAILURE RATE SOURCE (See Column 19)
A ATM 605A C _____
B _____ D _____

24 NOTE: DERATED VOLTAGE IS DETERMINED BY:
V_{MAX} = V_{NOM} * .8 (V_{RATED MAX} - V_{NOM})
V_{MIN} = V_{NOM} * .5 (V_{NOM} - V_{RATED MIN})

26 TOTAL FAILURE RATE .0120 %/1000 HRS

82A 679

PROJECT: LSG

ASSEMBLY: Board #8

SUBASSEMBLY: Stabilized Oscillator

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

[illegible]

BS-321A

-age 2 of 30

PROJECT: LSG
ASSEMBLY: Board #8

SUBASSEMBLY: Demodulator

DATE: 1/5/71
SCHEMATIC NO:

(Capacitors)

[illegible]

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CAPACITORS

SCHEMATIC NO: LGE-D4 2362312

[illegible]

BS-321A

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CAPACITORS

DATE: 1/5/71

SUBASSEMBLY: Command Counter

SCHEMATIC NO:

(Capacitors)

[illegible]

BS-321A

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PROJECT: LSG

ASSEMBLY: Board #2

SUBASSEMBLY: Command Decoder and Drive

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

[illegible]

BS-321A

PROJECT: LSG

ASSEMBLY: Board #1

SUBASSEMBLY: Dig. Mux Control

DATE: 1/5/71

SCHEMATIC NO:

[illegible]**BS-321A**

PROJECT: LSG

ASSEMBLY: Board #1

SUBASSEMBLY: Dig. Mux

DATE: 1/5/71

SCHEMATIC NO: 2362304

(Capacitors)

[illegible]

BS-321A

CAPACITORS

SCHEMATIC NO: 2362312

[illegible]

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PARTS APPLICATION ANALYSIS

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CAPACITORS

PROJECT: LSG

ASSEMBLY: Board #3

SUBASSEMBLY: Analog Output Buffer

DATE: 1/5/71

SCHEMATIC NO: 2362312

(Capacitors)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
CIRCUIT SYMBOL NUMBER	TYPE DESIGNATION (MIL or MFD) CONSTRUCTION	MANUFACTURER	CAPACITANCE VALUE	TOLERANCE	MANUFACTURER'S RATED VOLTAGE	DC PEAK VOLTAGE	OPERATING VOLTAGE	VOLTAGE RATIO OPERATING/ RATED	MAXIMUM DUTY CYCLE	BULK AIR TEMPERATURE (°C)	CIRCUIT FUNCTION OR APPLICATION	BASIC FAILURE RATE (1000 HRS)	TECHNICAL SPECIFICATIONS (SEE BELOW)	SPECIAL ENVIRONMENT (DETR)	FAILURE RATE MULTIPLIER	FINAL FAILURE RATE	TOTAL CAPACITOR COUNT PER TYPE	TOTAL FAILURE RATE (1000 HRS)	
C20	CKR06BX105K	Aerovox	1.0	+10	50	15	-	30%	1	50	Decoupling	A			.01			.0005	
C21	CKR06BX105K	Aerovox				5	-	10%											
C22	CKR06BX105K	Aerovox	1.0		50	15	-	30%			Decoupling								
C6	CKR11BX220K	Aerovox	22 PF		200	20		10%			Lag Compensation								
C7	CKR11BX220K	Aerovox																	
C8	CKR11BX220K	Aerovox																	
C9	CKR11BX220K	Aerovox																	
C10	CKR11BX220K	Aerovox																	
C11	CKR11BX220K	Aerovox																	
C12	CKR11BX220K	Aerovox	22 PF																
C13	CKR12BX390K	Aerovox	39 PF																
C14	CKR12BX390K	Aerovox																	
C15	CKR12BX390K	Aerovox																	
C16	CKR12BX390K	Aerovox																	
C17	CKR12BX390K	Aerovox																	
C18	CKR12BX390K	Aerovox																	
C19	CKR12BX390K	Aerovox	39 PF	+10	200	20		10%	1	50	Lag Compensation	A			.01			.0005	
20												21						22	
FAILURE RATE SOURCES (FOR COLUMN #14)												CALCULATED MTBF _____ HRS						TOTAL FAILURE RATE .0085 1000 HRS	
A ATM 605A B _____																			
C _____ D _____																			

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PROJECT: LSG

ASSEMBLY: Board #1 and #9

SUBASSEMBLY: A/D Converter

DATE: 1/5/71

SCHEMATIC NO: 2362300

(Capacitors)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CIRCUIT SYMBOL NUMBER	TYPE DESIGNATION (MIL OR MFR) CONSTRUCTION	MANUFACTURER	CAPACITANCE VALUE and	TOLERANCE	MANUFACTURER'S RATED VOLTAGE	OPERATING VOLTAGE	VOLTAGE RATIO, RATED	MAXIMUM DUTY CYCLE	BULK AIR TEMPERATURE (°C)	CIRCUIT FUNCTION OR APPLICATION	BASIC FAILURE RATE (1000 HRS)	FOR USE OF RELIABILITY DEPT	SPECIAL ENVIRONMENT (1000 HRS)	FAILURE RATE MULTIPLIER	FINAL FAILURE RATE	TOTAL CAPACITOR COUNT PER TYPE	TOTAL FAILURE RATE (1000 HRS)	
C ₂₁	CKR06BX105K	Aerovox	1.0	+10	50	15	30%	1	50	Decoupling	A			.01			.0005	
C ₁	CKR11BX220K		22 PF		200	20	10%			Lag Compensation								
C ₄	CKR11BX220K																	
C ₆	CKR11BX220K																	
C ₇	CKR11BX220K																	
C ₁₁	CKR11BX220K		22 PF															
C ₂	CKR12BX390K		39 PF															
C ₃	CKR12BX390K																	
C ₅	CKR12BX390K																	
C ₁₀	CKR12BX390K																	
C ₁₂	CKR12BX390K		39 PF		200	20	10%			Lag Compensation								
C ₀	CKR06BX105K		1.0		50	15	30%			Decoupling								
C ₁₃	CKR06BX105K					5	10%											
C ₁₄	CKR06BX105K					5	10%											
C ₁₅	CKR06BX105K	Aerovox	1.0	+10	50	5	10%	1	50	Decoupling	A			.01			.0005	

20

FAILURE RATE SOURCES (FOR COLUMN #14)

A. ATM 605A B. _____

C. _____ D. _____

21

22

CALCULATED MTBF _____ HRS

TOTAL FAILURE RATE .0075 1 1000 HRS

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PROJECT: LSG

ASSEMBLY: Board #2

SUBASSEMBLY: Dig. Time Buffers & Receivers

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

[illegible]

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PROJECT: LSG

ASSEMBLY: Board #15

SUBASSEMBLY: Temp. Monitor

DATE: 1/5/71

SCHEMATIC NO:

[illegible]

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PROJECT: LSG

SUBASSEMBLY: Tilt Servo

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

[illegible]

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PROJECT: LSG

ASSEMBLY: Board #13

SUBASSEMBLY: Fixed Gain Pre-amp

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

[illegible]

BS-321A

PROJECT: LSG
ASSEMBLY: Board #8

DATE: 1/5/71
SCHEMATIC NO:

[illegible]

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PROJECT: LSG

ASSEMBLY: Board #7

SUBASSEMBLY: Free Modes Filter

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

[illegible]

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PROJECT: LSG
ASSEMBLY: Board #8

SUBASSEMBLY: Stabilized Oscillator

DATE: 1/5/71
SCHEMATIC NO:

(Capacitors)

[illegible]

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PROJECT: LSG

ASSEMBLY: Board #8

SUBASSEMBLY: Lute Grater

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

[illegible]

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PROJECT: LSG

ASSEMBLY: Board #7

SUBASSEMBLY: Seismic Filter

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

[illegible]

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PROJECT: LSG

ASSEMBLY: Board # 5

SUBASSEMBLY: Screo Servo

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

BS-321A

DATE: 1/5/71

SUBASSEMBLY: Mass Changing Servo

SCHEMATIC NO:

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PROJECT: LSG

ASSEMBLY: Board #5

SUBASSEMBLY: Caging Control

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

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PROJECT: LSG
ASSEMBLY: Board #14

SUBASSEMBLY: Shaft Encoder electronics

DATE: 1/5/71
SCHEMATIC NO:

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PROJECT: LSG

ASSEMBLY: Board #15

SUBASSEMBLY: Instrument Housing Temp. Control

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

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PROJECT: LSG

ASSEMBLY: Board #10

SUBASSEMBLY: Power converter

DATE: 1/5/71

SCHEMATIC NO:

(Capacitors)

BS-321A

PROJECT: LSG
ASSEMBLY: Board #1

DATE: 1/5/71
SCHEMATIC NO:

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CAPACITORS

SUBASSEMBLY: Dig MUX Control

DATE: 1/5/71
SCHEMATIC NO:

ATM-979
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PROJECT: LSG
ASSEMBLY: Board #2

SUBASSEMBLY: Command Decoder & Driver

DATE: 1/5/71
SCHEMATIC NO:

(Capacitors)

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ge of _____

CAPACITORS

DATE 1/5/71

SUBASSEMBLY: Command Counter

SCHEMATIC NO: _____

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PROJECT: ISC
ASSEMBLY: Servo loop Module

SUBASSEMBLY: oscillator

DATE: 1/5/71
SCHEMATIC NO:

ATM-979
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PARTS APPLICATION ANALYSIS

Page 1 of 8(RELAYS)PROJECT: LSGDATE: 2/2/71ASSEMBLY: Board #15SUB ASSEMBLY: Inst. Housing Temp. ControlSCHEMATIC NO: 2362324

(Relays)

CIRCUIT REFERENCE DESIG- NATION	TYPE DESIGNATION (CEC, MIL OR MFR) AND CONSTRUCTION	MANUFACTURER	CONTACT LOAD							NUMBER OF POLES	RELAY COIL				RATE OF OPERA- TIONS PER HOUR OR SECOND	REQ'D LIFE OPERA- TIONS	MISCELLA- NEOUS REMARKS	ST T I M E I N T E R V A L S B E T W E E N F A I L U R E S (HRS)	S O F T T I M E I N T E R V A L S B E T W E E N F A I L U R E S (HRS)	F A I L U R E M O D E S (LOW)	TOTAL FAILURE RATE (%/1000 HOURS)	
			RATED		ACTUAL				TYPE OF L O A D		P O W E R	VOLTAGE		R E Q U I R E D L I F E O P E R A T I O N S P E R H O U R O R S E C O N D								
			V O L T A G E V	C U R R E N T A	VOLTAGE		CURRENT					M A X P O W E R W A T T E R E D M I N	M A X V O L T A G E V									M I N V O L T A G E V
					STEADY STATE	PEAK	STEADY STATE	SURGE														
K ₁	422D-12	Teledyne 40M47506 -33			28.95	29.6	.055	-		2	2	192 M	65 m	12	7					A	.0040	
24	DEVICE AVERAGE AMBIENT TEMPERATURE °C 50	FAILURE RATE SOURCES (FOR COLUMN NO. 21) A <u>ATM 605B</u> B _____ C _____ D _____								CALCULATED MTBF _____ HOURS				TOTAL FAILURE RATE _____ %/1000 HRS								
25										26				27								

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PARTS APPLICATION ANALYSIS

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(RELAYS)

PROJECT: LSG
ASSEMBLY: Board #15SUB ASSEMBLY: Sensor Assy. Heater Controller
Monitor Assy. SCHEMATIC NO: 2362381/2362395

DATE: 2/2/71

(Relays)

CIRCUIT REFERENCE DESIG- NATION	TYPE DESIGNATION (CRC, MIL OR MFR) AND CONSTRUCTION	MANUFACTURER	CONTACT LOAD						TYPE OF LOAD	NUMBER OF POLES		RELAY COIL				RATE OF OPERA- TIONS PER HOUR OR SECOND	REQ'D LIFE OPERA- TIONS	MISCELLA- NEOUS REMARKS	B F A I L U R E R E C O R D E D I N T H E F I L E S E E S E C T I O N 20	O F F M O D I F I E R	TOTAL FAILURE RATE (%/1000 HOURS)
			RATED		ACTUAL					T O T A L	A C T I V E	MAX R A T E D	A C T U A L	MAX P U L L I N G	MIN. O P E R. R.						
			V O L T A G E V	C U R R E N T A	VOLTAGE		CURRENT														
					STEADY STATE	PEAK	STEADY STATE	SURGE													
K ₁	422D-12	Teledyne 40M47506 -32			5V .1V		10 A 1 A	100 A		2	2	192 Min	65 Min	12	7					A	.0040
K ₂	422D-12																				
K ₃	422D-12																				
K ₄	422D-12																				
K ₅	422D-12																				
K ₆	422D-12	Teledyne 40M47506 -32			5V .1V		10 A 1 A	100 A		2	2	192 Min	65 Min	12	7					A	.0040

24	DEVICE AVERAGE AMBIENT TEMPERATURE °C 50	25	FAILURE RATE SOURCES (FOR COLUMN NO. 31) A ATM 605B B _____ C _____ D _____	26	CALCULATED MTBF _____ HOURS	27	TOTAL FAILURE RATE .0240 %/1000 HRS
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PROJECT: LSG
ASSEMBLY: Board #5

SUB ASSEMBLY: Caging Control

DATE: 2/2/71
SCHEMATIC NO:

[illegible]

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PARTS APPLICATION ANALYSIS

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(RELAYS)

PROJECT: LSG
ASSEMBLY: Board #4 and #5SUB ASSEMBLY: Screw ServoDATE: 2/2/71
SCHEMATIC NO: _____

(Relays)

CIRCUIT REFER- ENCE DESC- RIPTION	TYPE DESIGNATION (CBC, MIL OR MFR) AND CONSTRUCTION	MANUFACTURER	CONTACT LOAD						NUMBER OF POLES	RELAY COIL						MISCELLA- NEOUS REMARKS	B F A I L U R E S I L I N C U R R E N T S E E B E- L O W (3/ 1000 HRS) 20	S O F T M O D I F I E R	F R E Q U E N C Y H Z 21	T O T A L F A I L U R E R A T E (%/1000 HOURS) 23	
			RATED		ACTUAL					TYPE OF L O A D	POWER		VOLTAGE		RATE OF O P E R A T I O N S P E R H O U R O R S E C O N D 17						R E Q U I R E D L I F E O P E R A T I O N S 18
			V O L T A G E V 4	C U R R E N T A 5	V O L T A G E V 6	P E A K V 7	S T E A D Y S T A T E A 8	S U R G E A 9			M A X P O W E R W A T T E R 13	A C T U A L P O W E R 14	M A X V O L T A G E V 15	M I N V O L T A G E V 16							
K ₁	422D-12	Teledyne 40M47506 -33							2	2	192 Min	65 Min	12	7					A	.0040	
K ₂	422D-12	Teledyne 40M47506 -33							2	2	192 Min	65 Min	12	7					A	.0040	
DEVICE AVERAGE AMBIENT TEMPERATURE 50 °C			FAILURE RATE SOURCES (FOR COLUMN NO. 21) A <u>ATM 605B</u> B _____ C _____ D _____						CALCULATED MTBF _____ HOURS						TOTAL FAILURE RATE <u>.0080</u> %/1000 HRS						

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PARTS APPLICATION ANALYSIS

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(RELAYS)

PROJECT: LSG
ASSEMBLY: Board #4

SUB ASSEMBLY: Tilt Servo Control

DATE: 2/2/71
SCHEMATIC NO:

(Relays)

CIRCUIT REFER- ENCE DESIG- NATION	TYPE DESIGNATION (CEC, MIL OR MPR) AND CONSTRUCTION	MANUFACTURER	CONTACT LOAD							NUMBER OF POLES T O T A L	RELAY COIL							MISCELLA- NEOUS REMARKS	F A I L U R E R A T E (%/1000 HOURS)	
			RATED		ACTUAL				TYPE OF L O A D		POWER		VOLTAGE		RATE OF O P E R A T I O N S P E R H O U R S O R S E C O N D	REQ'D L I F E O P E R A T I O N S				
			V O L T A G E V	C U R R E N T A	VOLTAGE		CURRENT				M A X R A T E W A T T E R S I N T E N S I T Y	M A X P O W E R W A T T E R S I N T E N S I T Y	M A X V O L T A G E	M I N V O L T A G E						
					STEADY STATE	PEAK	STEADY STATE	SURGE												
K ₁	422D-12	Teledyne 40M47506 -33								2	2	192	65	12	7				A	.0040
K ₂	422D-12	↓								↓	↓	↓	↓	↓	↓				↓	↓
K ₃	422D-12	Teledyne 40M47506 -33								2	2	192	65	12	7				A	.0040
24	DEVICE AVERAGE AMBIENT TEMPERATURE 50 °C		FAILURE RATE SOURCES (FOR COLUMN NO. 21) A ATM 605B B _____ C _____ D _____							CALCULATED MTBF _____ HOURS							TOTAL FAILURE RATE .0120 %/1000 HRS			

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PROJECT: LSG
ASSEMBLY: Board #7

SUB ASSEMBLY: Seismic Amp. & Filter

DATE: 2/2/71
SCHEMATIC NO:

(Relay)

[illegible]

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PARTS APPLICATION ANALYSIS

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(RELAYS)

PROJECT: LSG
ASSEMBLY: Board #8

SUB ASSEMBLY: Stabilized Osc.

DATE: 2/2/71
SCHEMATIC NO:

(Relays)

CIRCUIT REFERENCE DESIGNATION	TYPE DESIGNATION (CSC, MIL OR MFR) AND CONSTRUCTION	MANUFACTURER	CONTACT LOAD							NUMBER OF POLES T O T A L	RELAY COIL							MISCELLANEOUS REMARKS	TOTAL FAILURE RATE (%/1000 HOURS)				
			RATED		ACTUAL				TYPE OF LOAD		POWER		VOLTAGE		RATE OF OPERATIONS PER HOUR OR SECOND	REQ'D LIFE OPERATIONS							
			V O L T A G E V	C U R R E N T A	VOLTAGE		CURRENT				M A X R A T E D	A C T U A L	M A X M I N.	P U L S E									
					STEADY STATE	PEAK	STEADY STATE	SURGE															
K ₁	422D-12	Teledyne 40M47506 -33									2	2	192 Min	65 Min	12	7						A	.0040
24 DEVICE AVERAGE AMBIENT TEMPERATURE 50 °C	25 FAILURE RATE SOURCES (FOR COLUMN NO. 21) A ATM 605 B _____ C _____ D _____									26 CALCULATED MTBF _____ HOURS									27 TOTAL FAILURE RATE .0040 %/1000 HRS				

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PARTS APPLICATION ANALYSIS

Page 8 of 8(RELAYS)PROJECT: LSGDATE: 2/2/71ASSEMBLY: Board #8SUB ASSEMBLY: Demod-Integrator

SCHEMATIC NO: _____

(Relays)

CIRCUIT REFERENCE DESIGNATION	TYPE DESIGNATION (CEC, MHL OR MPR) AND CONSTRUCTION	MANUFACTURER	CONTACT LOAD								NUMBER OF POLES	RELAY COIL				RATE OF OPERATIONS PER HOUR OR SECOND	REQ'D LIFE OPERATIONS	MISCELLANEOUS REMARKS	FAILURE RATE (%/1000 HOURS)	TOTAL FAILURE RATE (%/1000 HOURS)		
			RATED		ACTUAL				TYPE OF LOAD	POWER		VOLTAGE										
			V O L T A G E V	C U R R E N T A	VOLTAGE		CURRENT			MAX R A T E W A T T E R E D		A C T U A L	MAX P U L S E V O L T A G E V	MIN O P E R A T I O N A L V O L T A G E V								
					STEADY STATE	PEAK	STEADY STATE	SURGE														
K ₁	422D-12	Teledyne 40M47506 -33									2	2	92 Min	65 Min	12	7					A	.0040
DEVICE AVERAGE AMBIENT TEMPERATURE 50 °C			FAILURE RATE SOURCES (FOR COLUMN NO. 21) A <u>ATM 605B</u> B _____ C _____ D _____								CALCULATED MTBF _____ HOURS				TOTAL FAILURE RATE <u>.0040</u> %/1000 HRS							

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PART DESCRIPTION	MFG. PART NO.	RELIABILITY SOURCE REF.	% OF RATED TORQUE	% OF RATED CURRENT	°C OPERATING TEMP.	FAILURE RATE % / 1.000 HRS.
1 Connector	Cannon DDH 50 P	Farada (1A)p. 2.73	50	50	50	.02
Connector leads (solder joints)	Cannon DBH 25 P	Farada (1A)p. 2.73	50	50	50	.02
		MIL-HDBK-217A p. 7.11-1			50	.00020
2 Arrestment Motor	Globe 43A146-2	Farada (1A) p. 2.133	33		50	1.43
3 Clutch	PIC T18-3	Farada (1A) p. 2.432	32		50	.0507
3 Ball Bearings		Farada (1A) p. 2.411			50	.0532
4 Pin Stop Drive	ADL				50	
5 Mass Changing Motor	Globe 128A174-11	Farade(1A) 1. 2.133	33		50	1.43
6 O-Ring Clutch	ADL	Est. 3 x 10	32		50	.507
7 Gears		Farada (1B) p. 2.411			50	.358
Bearings		Farada (1A) p. 2.411			50	.0532
8 Potentiometer	Bourns # 37005-1-104	Farada (1A) 1. 2.186			50	.591
9 Mass Changing Limit Stop	ADL				50	
10 Coarse Screw Motor	IMC 008-949	Farada (1A) p. 2.133	12		50	.175

PART DESCRIPTION	MFG. PART NO.	RELIABILITY SOURCE REF.	% OF RATED TORQUE	% OF RATED CURRENT	°C OPERATING TEMP.	FAILURE RATE %/ 1,000 HRS.
11 Clutch Gears & Bearings	See 3 & 7		32		50	.462
12 Revolution Counter (STOP)		Farada p. 2.448			50	.507
13 Fine Screw Motor	IMC 008-949	Farada 1A p. 2.133	12		50	.175
14 Clutch Gears & Bearings	See 11		32		50	.462
15 Revolution Counter	Same as 12				50	.507
16 Leveling Motors	IMC 008-845-24				50	.175
17 Gimbal Suspension					50	0
18 Thermal Control	Heater Box Heater 1680-1800 r	Farada 1B p. 2.499	60	60	50	.019
18	Instru. H's'g Heater 104-108 r	Farada 1B	1.2 Night 80% 22 Day 3%	1.2 Night 80% 22 Day 3%	50	.019
18	Survival Heater 192-196 r	Farada 1B p. 2.499			50	.019
18 Heater Potting Material					50	0
18 Instrument Hsg. Insulation		Farada 1B p. 2.520			50	0

ADL - PARTS APPLICATION ANALYSIS (cont)

PART DISCRIPTION	MFG PART NO.	RELIABILITY SOURCE REF.	% OF RATED TORQUE	% OF RATED CURRENT	°C OPERATING TEMP.	FAILURE RATE %/1,000 HRS
19 Pressure Control	O-Ring				50	0
19 Thermistor	Yellow Springs Inst. Co	Farada 1 B p. 2.598			50	.077
20 Fine & Coarse	Librascope	Farada 1 B			50	1.482 (LT)
21 Screw ENCODERS	719-11-5	p. 2.563				